ENGINEERING REFERENCE SPECIFICATION

2100 UNIVERSAL INTERFACE BOARD

(12930A)

J. S. Toreson
February 24, 1972

Introduction

The Universal Interface (UI) is functionally an extension of the basic microcircuit interface with additional features allowing it to cover applications requiring the following:

1. Wide peripheral - CPU separation through the use of differential I/O transmission.
2. Successive cycle steals under DMA.
3. Separately addressable and interruptable control and data channels.
4. Complete program control of the control channel handshaking sequence.
5. System 3000 - 2100 Interface.
6. 2610 & 2614 Line Printer Interface.*

*See separate ERS "2100 Interface to the 2610A, 2614A Line Printers."

To allow the control and data channels to operate independently, two select codes are used (SC_i and SC_{i+1}). This feature is switch programmable, and if selected the I/O slot (i+1) must have a jumper card installed in it if the priority chain is to be continued.

This ERS is organized as follows:

I. Block Diagram and Description.

II. Control - Data Flow.

III. General Specifications.

IV. Figures and Tables.

I. Block Diagram

In Figure 1 a block diagram of the UI is given. The lower select code (LSC) blocks are associated with the data channel, and the higher select code (HSC) blocks are associated with the optional, independently addressable control channel. A functional description of each block is given in this section. The data and control flow, and their word formats, are defined in the next section.

LSC Flag and Control Circuit

A simplified logic diagram of this circuit appears in Figure 2. This portion of the UI is functionally equivalent to the control section of the standard microcircuit interface. The main difference is the definition of the Service Request (SRQ) signal.

The new definition of the SRQ signal is required to allow high-speed DMA transfers up to 1 megaword/second. SRQ was derived from the FLAG FF which is contained within the interrupt/flag block shown in Figure 2. This resulted in an SRQ signal which came too late to request the next cycle, constraining DMA rates to less than 500 kilowords/sec. This situation is alleviated by taking the SRQ signal from the Flag Buffer FF, which allows the I/O device-UI handshaking signals enough time to request the next successive cycle, and thereby accomplishes the maximum transfer rate of 1 M word.

It should be noted that the Flag Buffer FF, hence the SRQ signal, can be set asynchronously. The signal will be synchronized, however, on the DMA card by the cycle request FF.

The maximum burst rate of 1 M word does not imply that DMA transfers can proceed at a variable, synchronous

rate to 1 M word. If synchronous operation is required, additional word buffering must be provided by the I/O device. The timing of DMA transfers is given in Figure 8, which illustrates the maximum allowable delays on the device command-device flag signal sequence to effect successive cycle steals.

Further details of this circuit block are omitted here due to its similarity to the existing microcircuit boards. The switch programmable options shown in Figure 2 are functionally defined in Table 1.

HSC Flag and Control Circuit

A simplified logic circuit of this circuit appears in Figure 3. This circuit is also similar to the control section of a standard microcircuit card. The two main differences are as follows:

1. No DMA capability. This is due to lack of an SRQ_{i+1} output signal at the ith I/O card slot.
2. Select code inhibit switch.

The switch programmable options shown in Figure 3 are functionally defined in Table 2.

LSC Output Register

This block is shown in Figure 4 and consists of a 16 bit edge strobed register, which loads the IOBO bus lines at the trailing edge of IOO. The register outputs then pass directly to ungated differential line drivers. It should be noted that the differential drivers used do not support "party line" operation.

LSC Input Register

This block is also shown in Figure 4, and consists of a 16 bit edge strobed register, which is loaded by the input strobe signal derived from Figure 2. The register loads data from the differential line receivers,

which nterface the I/O signals to the required TTL levels. The source of the signal for Bit 0 can be selected (See Table 3 Switch 102S1) from either the I/O device Bit 0 or the L Dev FLG composite signal as shown in Figure 4. This allows the device flag signal to be used as a busy status indicator which is required in some applications (e.g., line printer). When the switch is in this position, the I/O device Bit 0 input should be left open.

HSC Input/Output Circuit

This circuitry constitutes the secondary "control channel." The output control register (CR) consists of six bits and is illustrated in the Block Diagram (Figure 1) and also in a simplified logic diagram in Figure 5. The register is loaded from the IOBO lines similar to the LSC output register described above. The six inbound status lines are gated (not stored) onto the IOBI lines during an LI* (HSC) instruction. This requires that the status information be continuously available.

Miscellaneous Programmable Control Functions

These switches appear in the schematic in Figure 5 and are listed in a function table in Table 3.

Two of these switches (85S3 and 85S2) give flexibility in the HSC "control channel" by modifying the logical definition of the 6 bit command word lines (CW15-CW10) and the HSC device command signals. The control flow details are prescribed in the next section.

Switch 102S3 is used to allow the "oring" of the H Dev FLG and the L Dev FLG signals. The use of this is outlined in the aforementioned line printer ERS.

Power On (PON) Circuit

This circuit is shown in Figure 10. The design criteria are as follows:

1. Common mode voltage (CMV) rejection should be as high or higher than that of the differential driver-receiver pair (±15 volts).
2. Speed should be commensurate with the power failure warning time (total = 500 μs.)
3. Throughout the power failure the PON logic must faithfully transmit the impending power failure.
4. Any circuit burden to be borne by the UI (i.e., the user should not have to buy any exotic parts to interface to it.)
5. Use a maximum of 2-I/) connector pins for both outbound transmission of impending UI power failure and inbound detection of an I/O device power failure.

The circuit shown consists of a "current loop", transmitted via twisted pair, which originates and terminates only at the I/O device. This results in high common mode voltage rejection which discriminates against ground offsets and ground noise amplitudes up to several hundred volts. The twisted pair reduces the loop flux linkage area, and its attendant non-common mode induced voltage to a minimum.

The circuit operation can be partitioned into the following stages:

A) The current is sourced from the I/O device (PON IN) by a suitable current sourcing circuit (e.g. emitter follower, Signetics 8T23, CTL, etc.)

B) The 2100 PON signal "makes" the opto-isolator switch (OI-1).

C) Current detection is accomplished by OI-2, which outputs a logic "1" for zero loop current (power system failure).

D) The current is transmitted to the I/O device (PON OUT) and terminates in a current detector (e.g. open base, Signetics 8T24, CTL, etc.)

II. "Control" and "Data" Channel Word Formats

The "data" channel or LSC outbound word passes from the CPU to the device unaltered. The inbound word does have an aforementioned Bit 0 option, which is the selection of L Dev CMD signal instead of the I/O device input Bit 0.

The "control" channel described from a circuit viewpoint in the previous section is illustrated from a software word viewpoint in Figures 6 and 7. Figure 6 shows the output word layout and a logical definition of each bit position. Similarly in Figure 7, a definition of each bit position is given for the inbound word. These definitions are self-explanatory, but it should be noted that the current contents of the control register are available left-justified in the control channel input word. Thus a permanent "loop back" capability exists on the UI for the control channel. In addition to a "loop back" capability, this feature allows the current "state" of the interface to be analyzed by one . LI* (HSC) instruction (i.e., a memory read may not have to be made to determine the current state that the operating software has placed the link into).

A complete logical definition of the I/O device signal lines also appears in Figures 6 and 7.

III. General Specifications

I/O Device - UI Signal Transmission

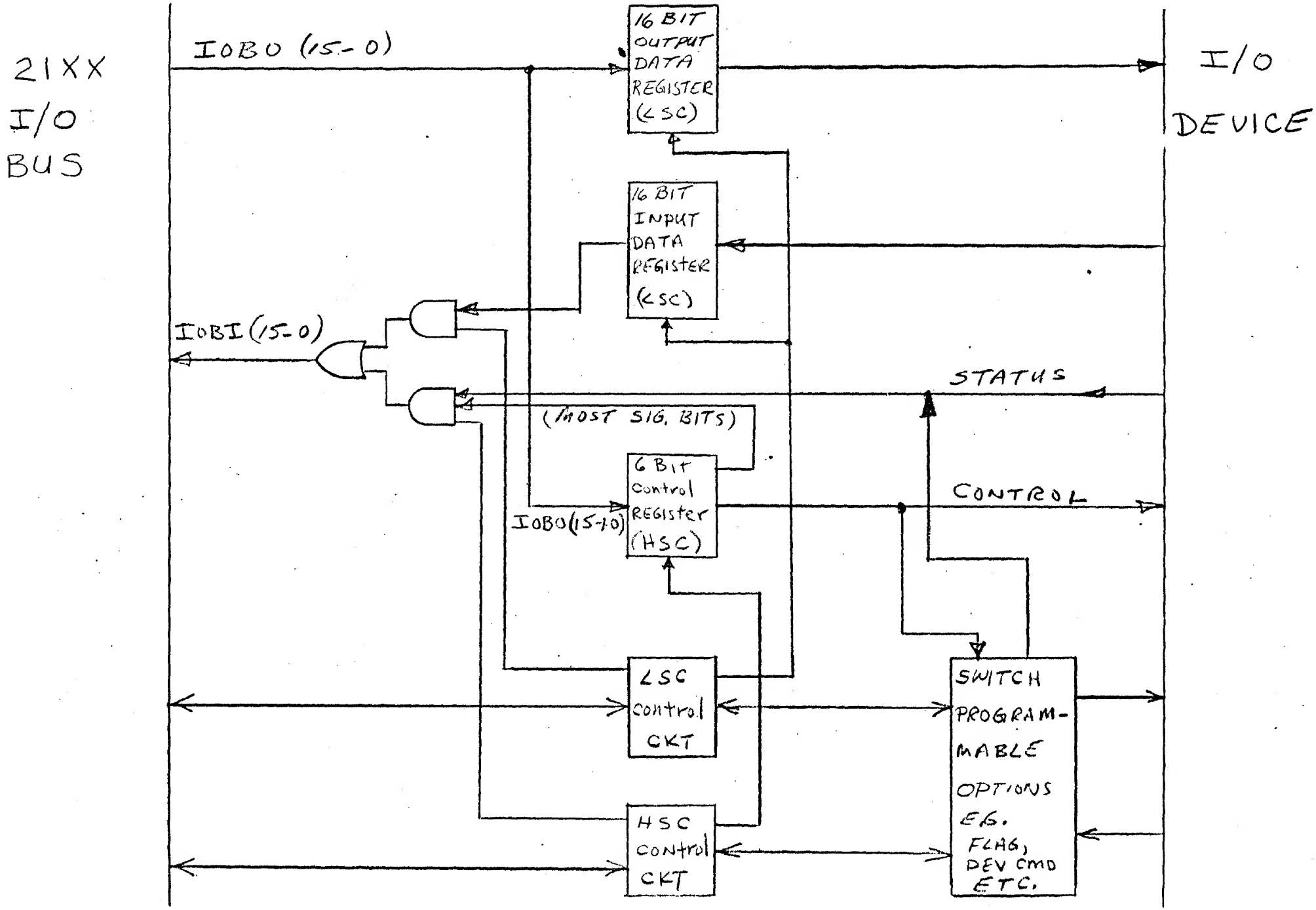
One basic UI circuit board interfaces between the following three signalling schemes: 1) differential; 2) positive true TTL; 3) negative true TTL. This is accomplished by three different loadings of resistive bias-terminating networks. A logic-schematic of each of the above three configurations appears in Figures 11, 12 and 13. The signal loading-driving characteristics are also given in the Figures.

I/O Power Supply Loading

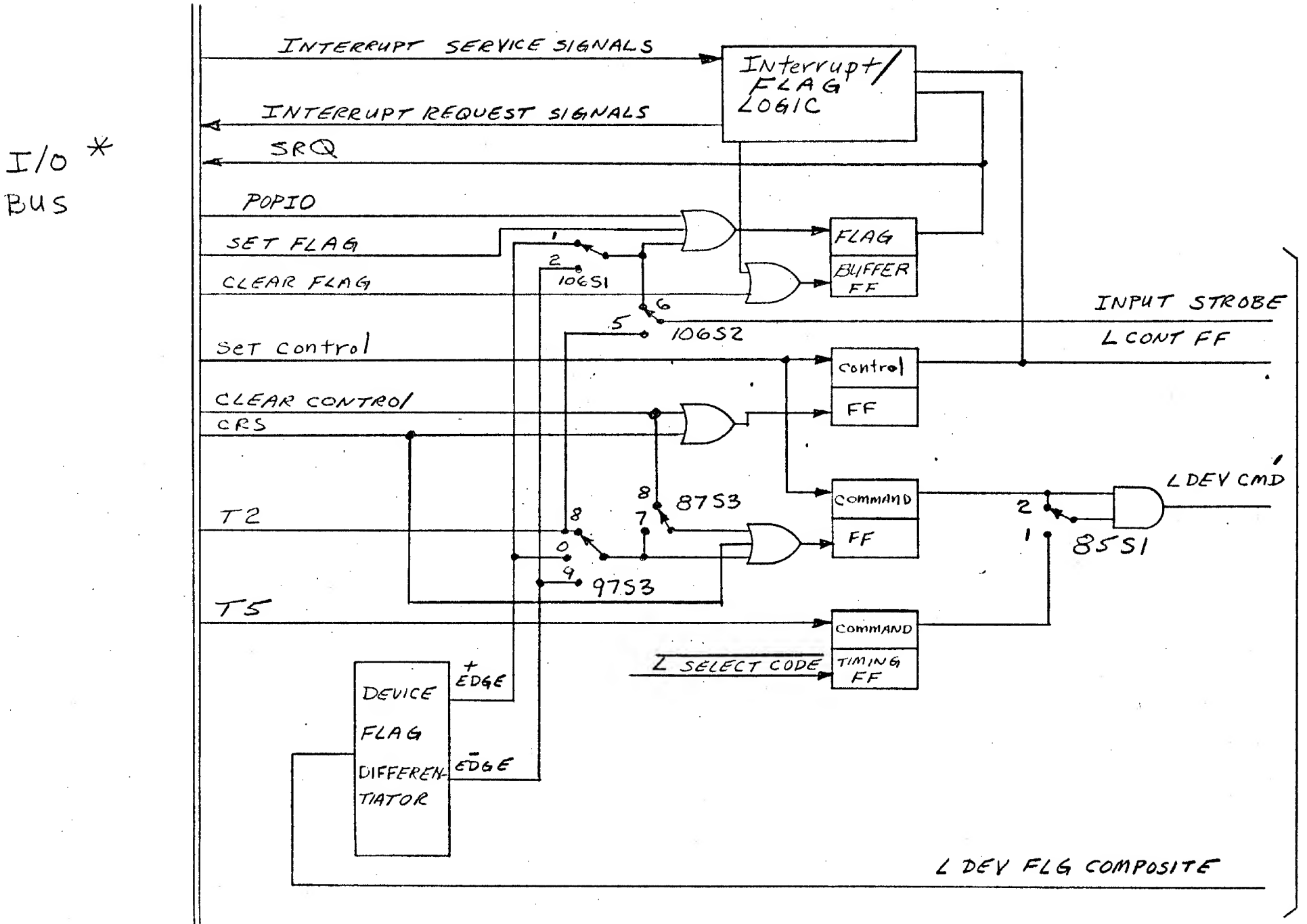
In Figure 14 the power supply loading is given for all three configurations (differential, $\pm$ TTL). The following assumptions are implied by the calculated figures shown in the Figure:

1. Board fully loaded.
2. I/O - UI signals are in a 50% on-off duty cycle.
3. Worst case power consumption on each chip.

IV. Figures and Tables



Universal Interface - Block Diagram



* Note: SIGNAL DEPENDENCY ON Select CODE IS implied IN ALL OF THE ABOVE APPROPRIATE SIGNALS

FIGURE 2 - LOWER SELECT CODE SIMPLIFIED CONTROL LOGIC

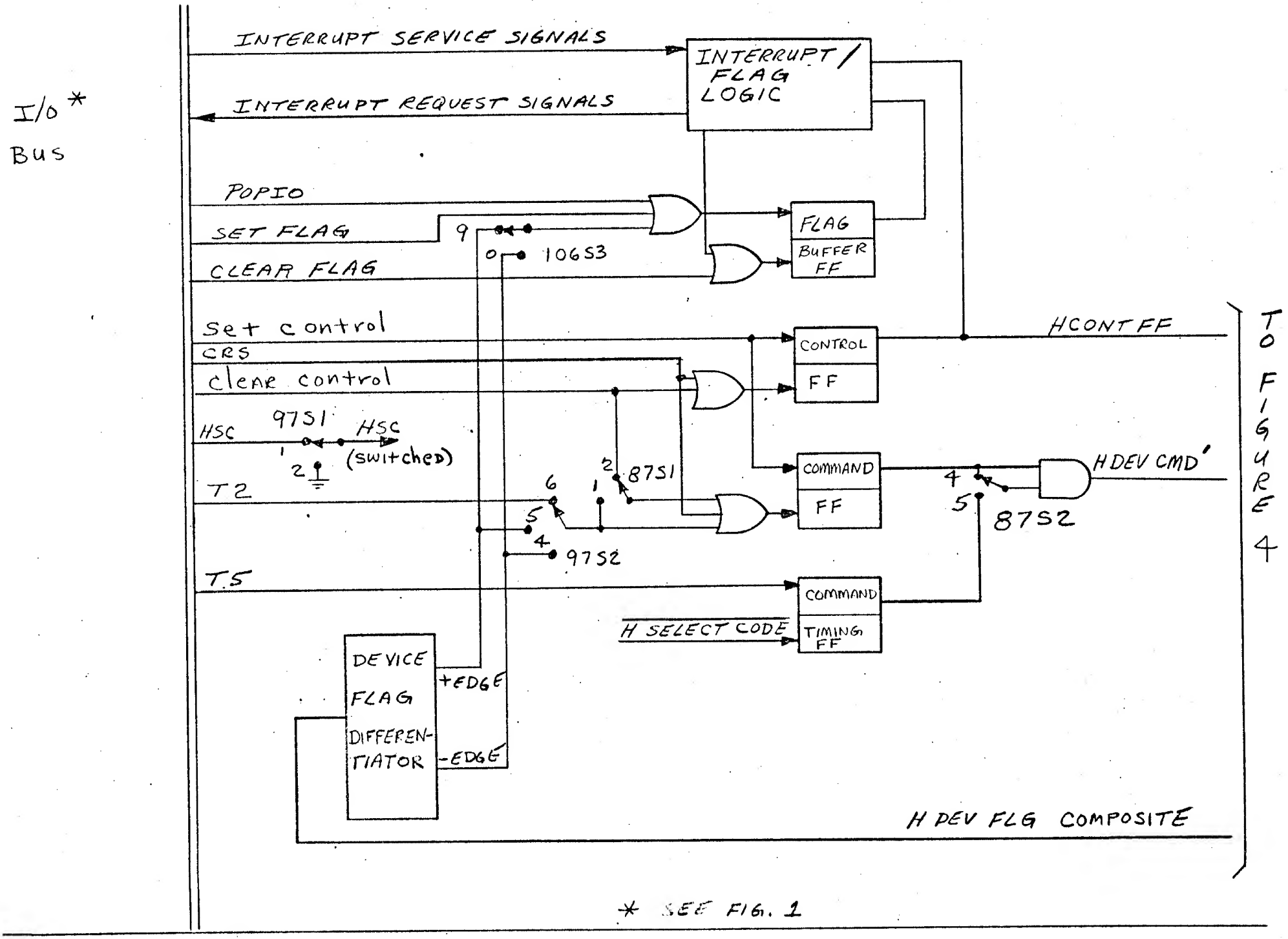
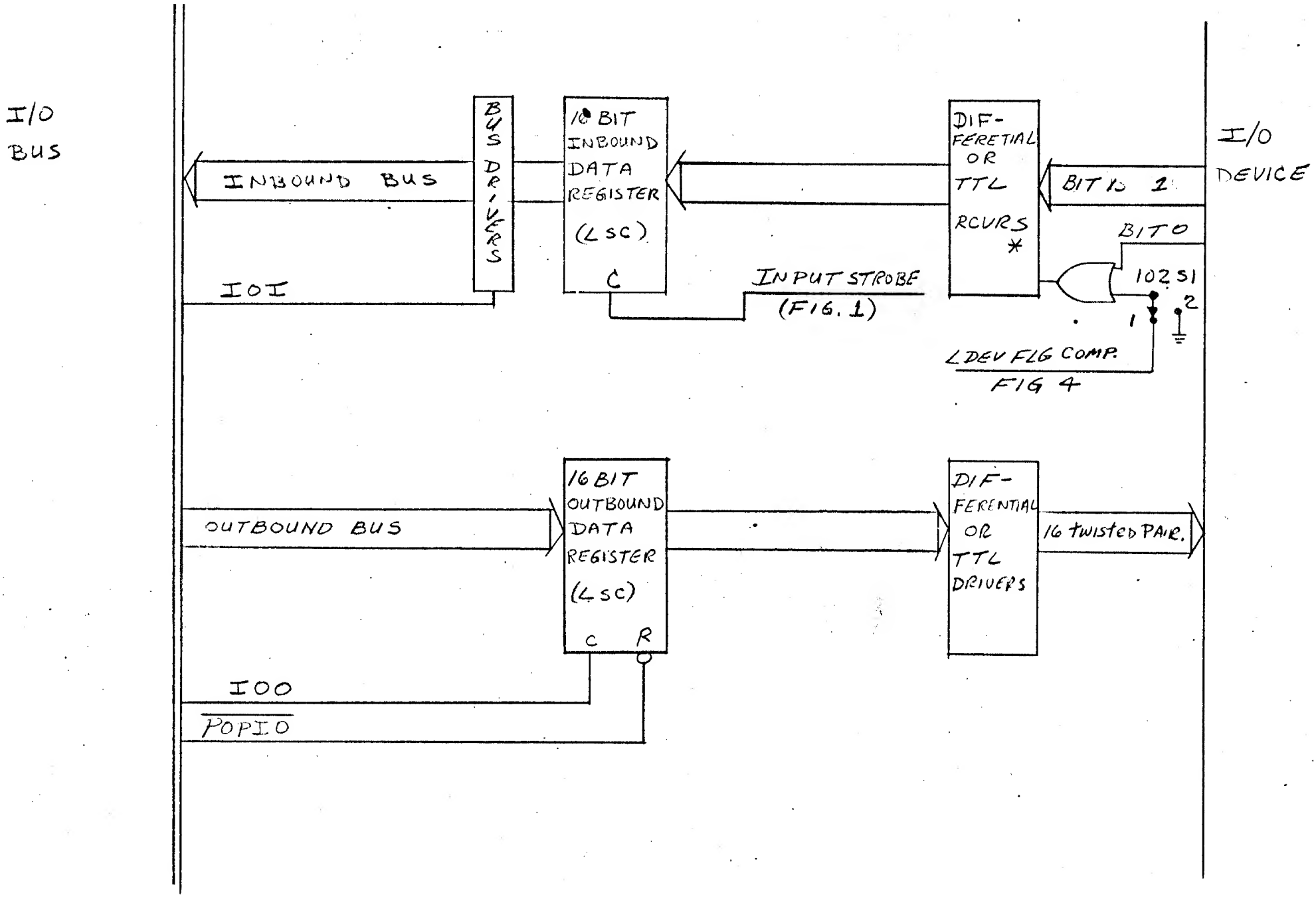


FIGURE-5 HIGHER SELECT CODE SIMPLIFIED CONTROL LOGIC



* SAME CIRCUIT HANDLES BOTH. FOR TTL RESISTORS ARE ADDED

FIGURE 4 - LSC INBOUND/OUTBOUND DATA FLOW

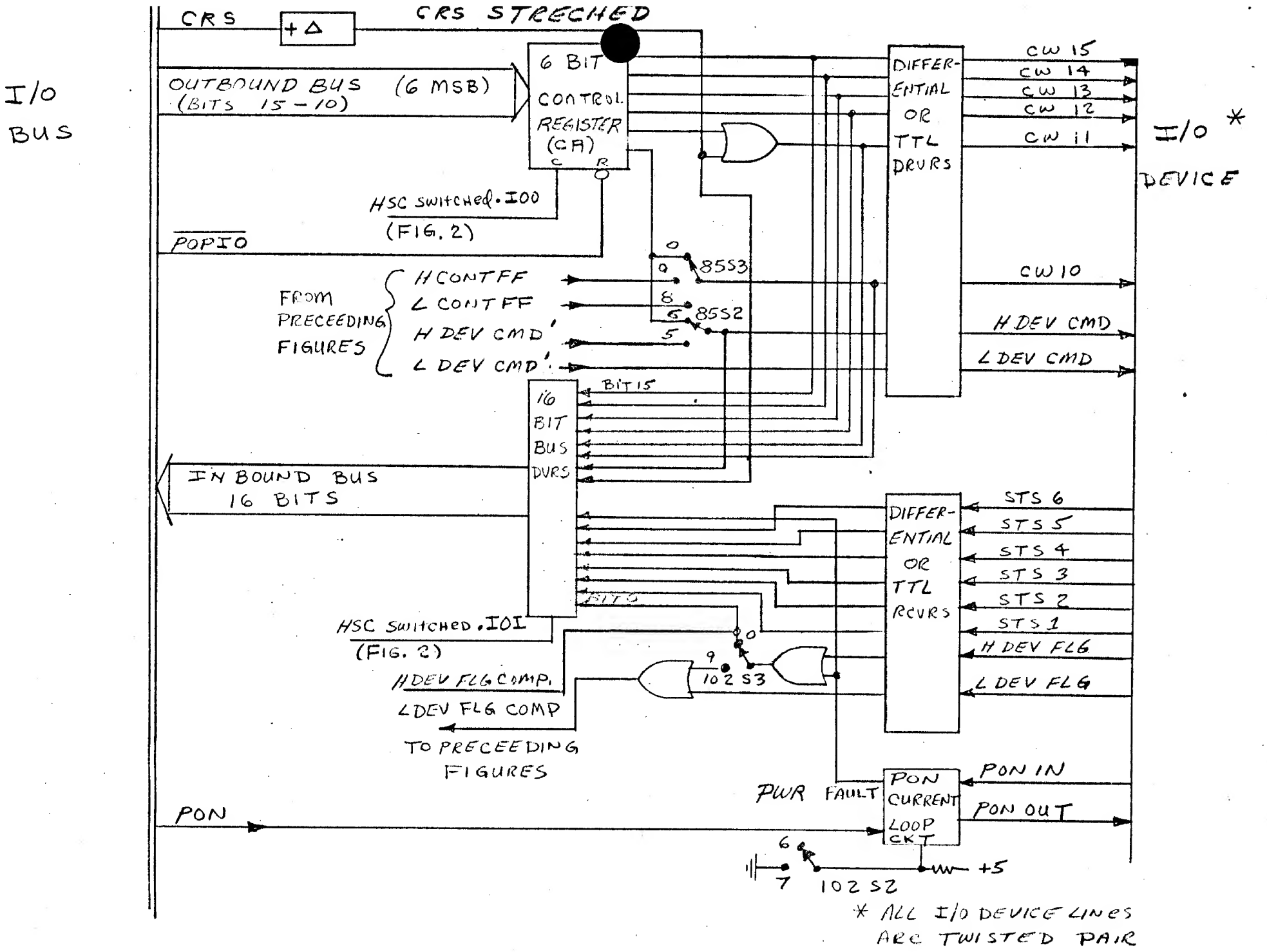
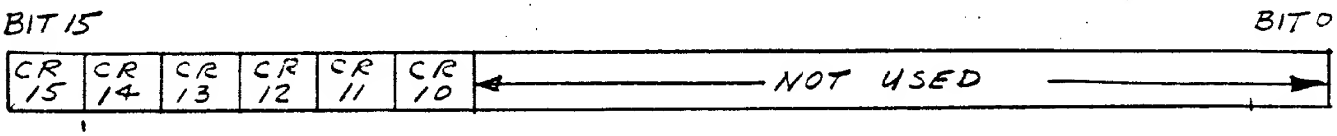


FIGURE 5 - HSC CONTROL AND STATUS CHANNEL, MISC. GATING (SIMPLIFIED)

CONTROL CHANNEL OUTPUT REGISTER (CR) FORMAT - (HSC)



(a.)

I/O DEVICE OUTPUT SIGNAL LINE DEFINITION

I/O OUTPUT

SIGNAL NAME	SIGNAL LOGICAL DEFINITION & SOURCES
CW 15	CONTROL REGISTER BIT 15 (CR 15)
CW 14	CR 14
CW 13	CR 13
CW 12	CR 12
CW 11	CR 11 + CRS STRECHED
CW 10	CR10 · 8553-0* + H CONT FF · 8553-9 + L CONT FF · 8553-8
H DEV CMD	CR10 · 8552-6 + H DEV CMD' · 8552-5
L DEV CMD	L DEV CMD'
PON OUT	POWER ON CURRENT LOOP. CURRENT ⇒ ALL PWR UP

(b)

* SWITCH 8553, IN INDEX POSITION 0 (See FIG. 9)

FIG. 6 OUTBOUND CONTROL INFORMATION FUNCTIONAL SPECIFICATION

CONTROL CHANNEL INPUT WORD FORMAT - (HSC)

BIT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	BIT 0
CW15	CW14	CW13	CW12	CW11	CW10	H DEV CMD	CRS STR.	P ON	STS 6	STS 5	STS 4	STS 3	STS 2	STS 1	H DEV FLG COMP

"LOOPBACK" OF OUTBOUND SIGNALS SEE FIG. 5

CRS STRECHED

I/O INPUT LINES DEFINED BELOW

(a)

H DEV FLG COMPOSITE = PWR FAULT + H DEV FLG

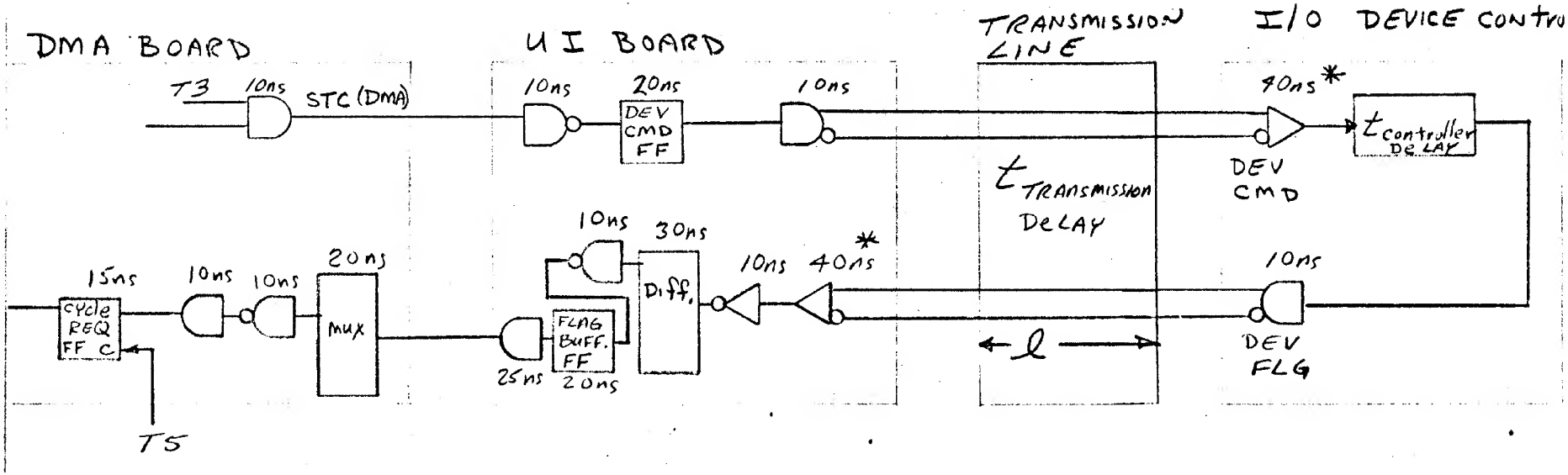
I/O DEVICE INPUT SIGNAL LINE DEFINITION

I/O INPUT SIGNAL NAME	SIGNAL DEFINITION	SIGNAL DESTINATIONS
PON IN	PON CURRENT LOOP	PON CURRENT DETECTER
STS 6	USER DEFINED STATUS	CONTROL CHANNEL INPUT WORD (a)
STS 5	" " "	" " " "
STS 4	" " "	" " " "
STS 3	" " "	" " " "
STS 2	" " "	" " " "
STS 1	" " "	" " " "
H DEV FLG	" " " /OR XFER COMPLETE-HSC	" " " /OR HSC FLAG CKT
L DEV FLG	XFER COMPLETE HSC	LSC FLAG CKT
GND	GND	GND

(b)

FIG. 7 INBOUND CONTROL (STATUS) INFORMATION

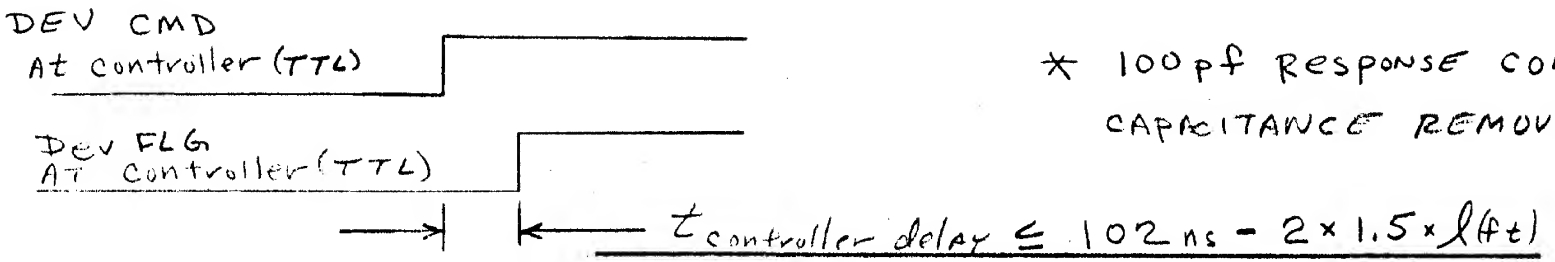
FUNCTIONAL SPECIFICATION



(a) Simplified LOGIC PATH showing DELAY CONTRIBUTING Elements (2100).

Timing Constraint: Loop must be traversed IN 2 time periods, i.e. T3 - T5

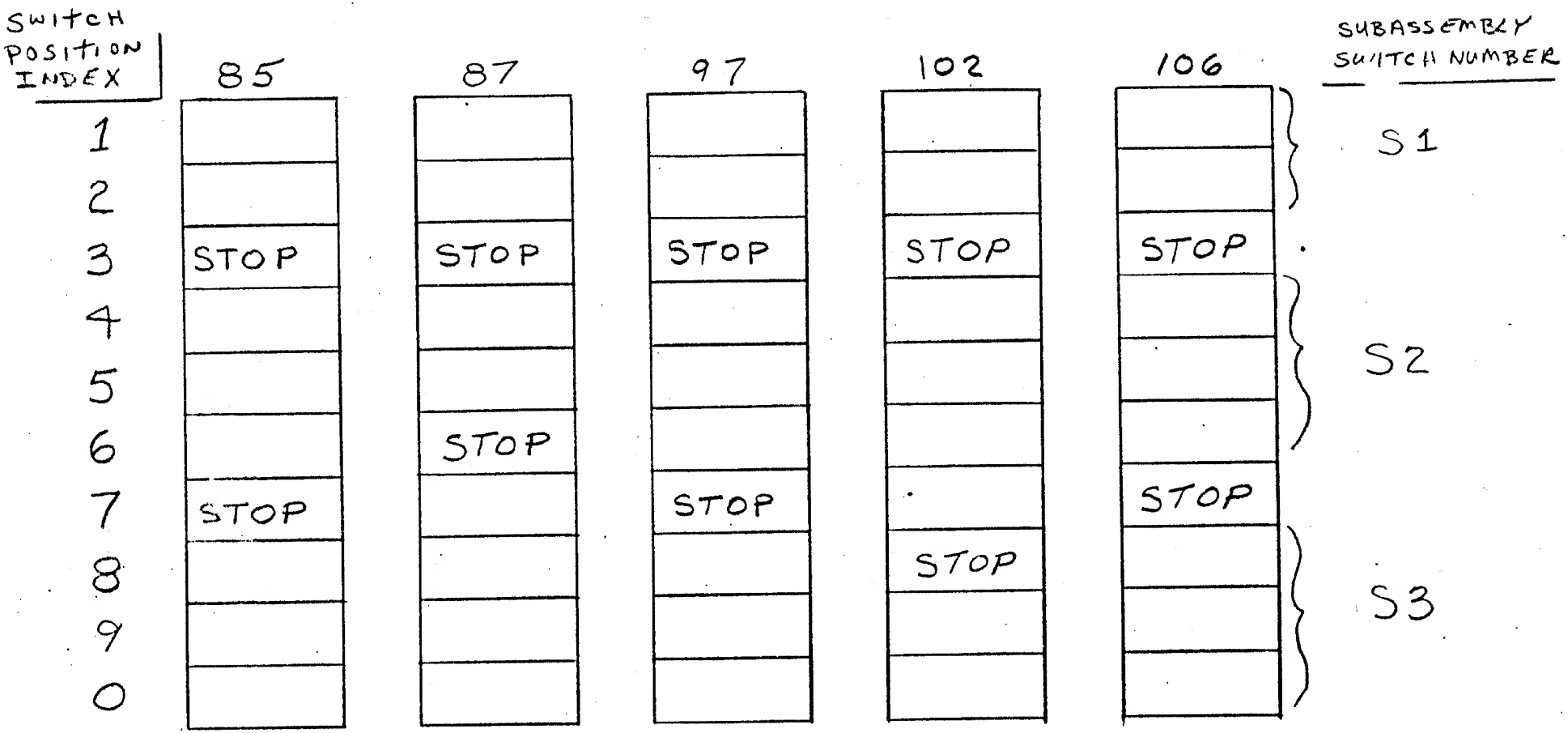
OR: $2t_{transmission\ DelAy} + t_{device\ controller} < 2 \times 196ns - 290ns = 102ns$



* 100pf RESPONSE CONTROL CAPACITANCE REMOVED

FIGURE 8 DMA Timing Constraints FOR Succesive cycle steals

SWITCH ASSEMBLY NUMBER - LOCATION CODE *



* NOTE; AN INDIVIDUAL SWITCH IS REFERRED TO BY A CONCATENATION OF ITS ASSEMBLY NUMBER AND SWITCH NUMBER, (E.G. 8551-2 ⇒ SWITCH NUMBER 2 IN INDEX POSITION 2, OF THE SWITCH ASSEMBLY LOCATED IN THE 8th ROW - 5th COLUMN

FIG. 9 DEFINITION OF PROGRAMMING SWITCH NOMENCLATURE

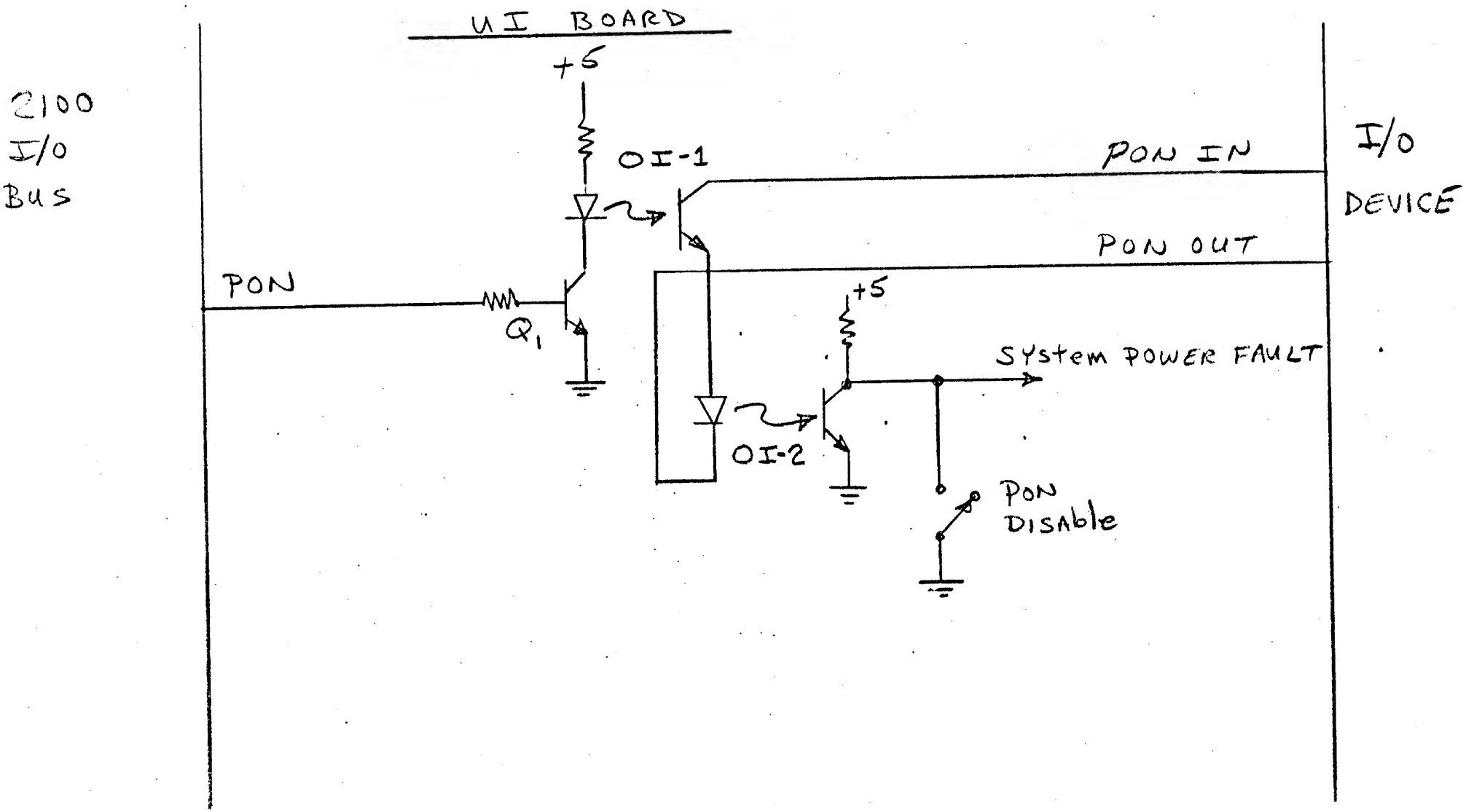
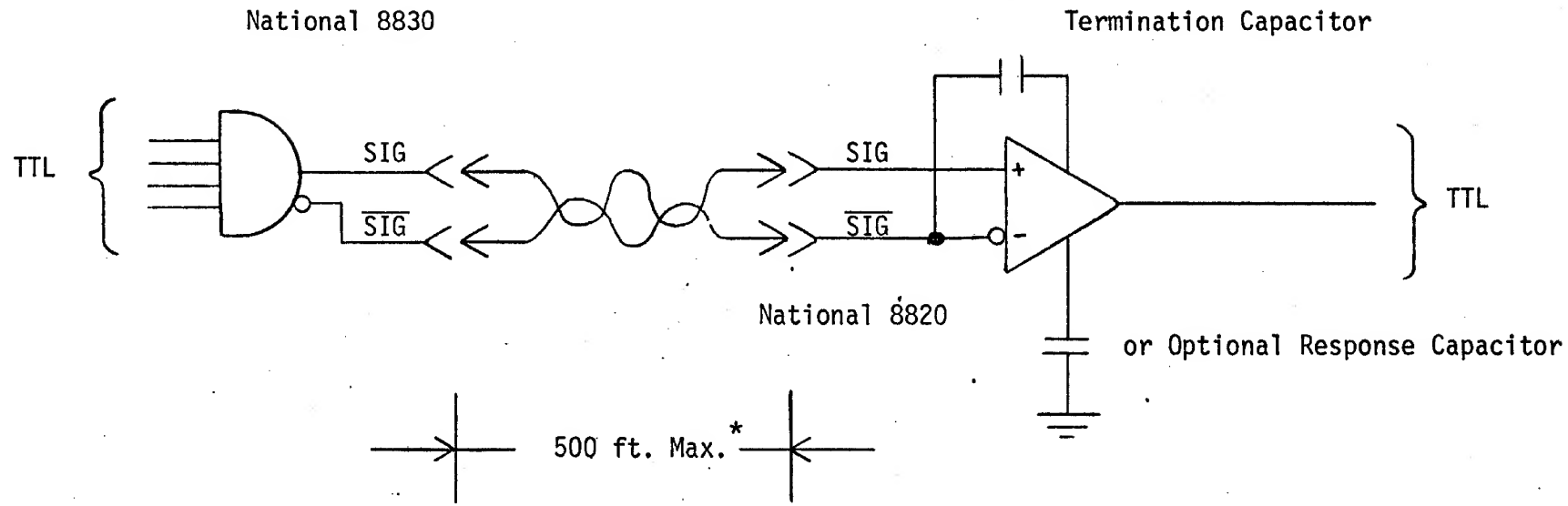


FIG. 10 POWER ON (PON) CIRCUITRY



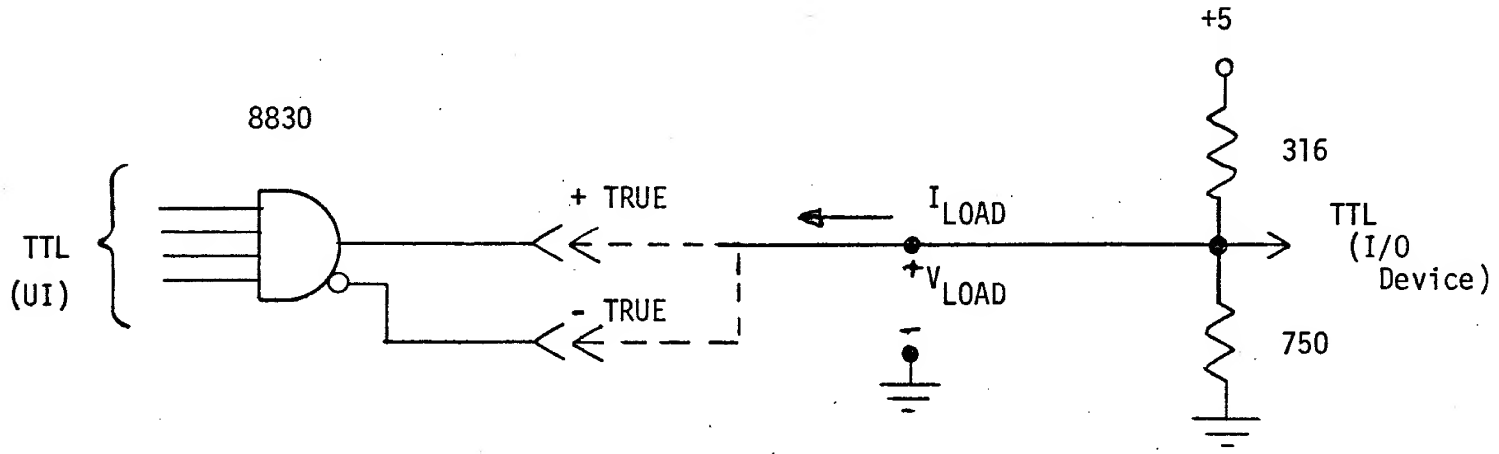
Signal Characteristics

Common mode voltage rejection = ± 15 volts.

Differential driver delay (load impedance 100Ω in series with 5000 pf) = 16ns W.C.

*note: This is the distance recommended in the CDC Line Printer Manual.

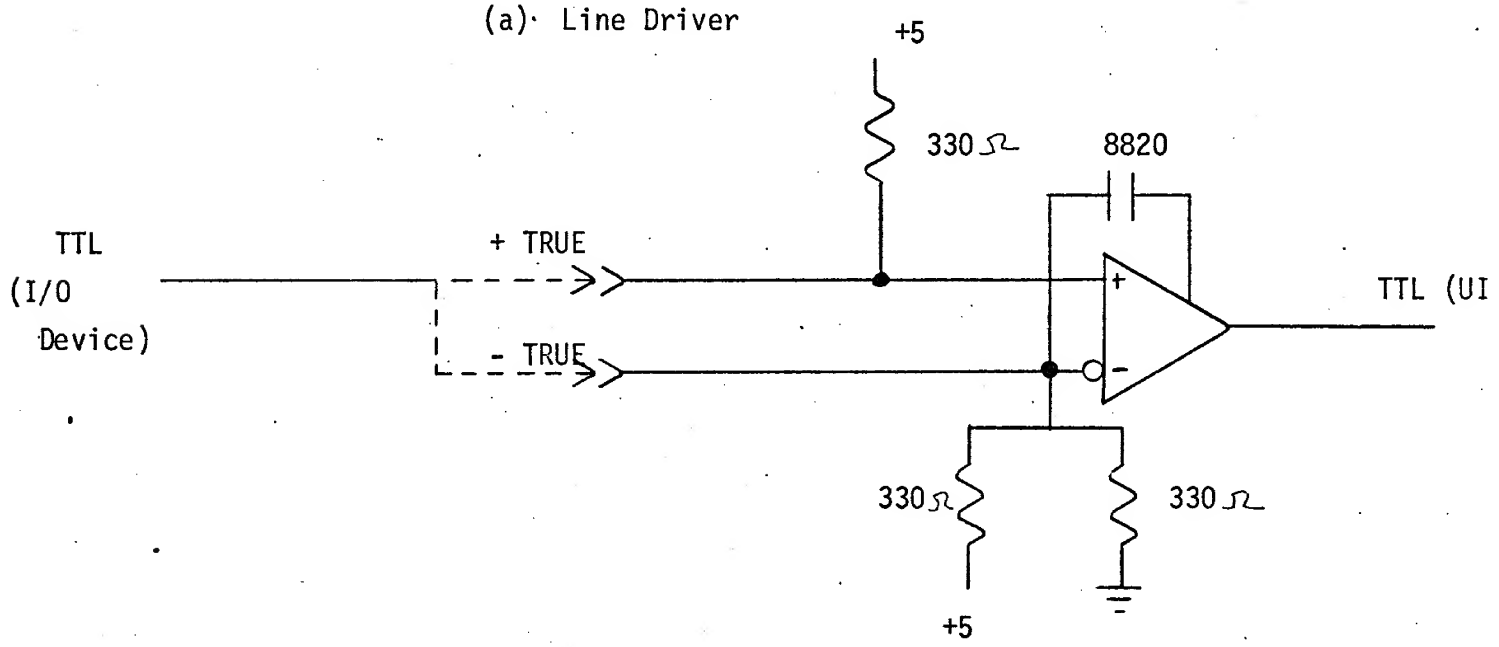
Figure 11 - Differential Transmission



V_{LOAD} Max. = .4 volt @ I_{LOAD} = 32mA

V_{LOAD} Min. = 2.0 volts @ I_{LOAD} = -.8mA

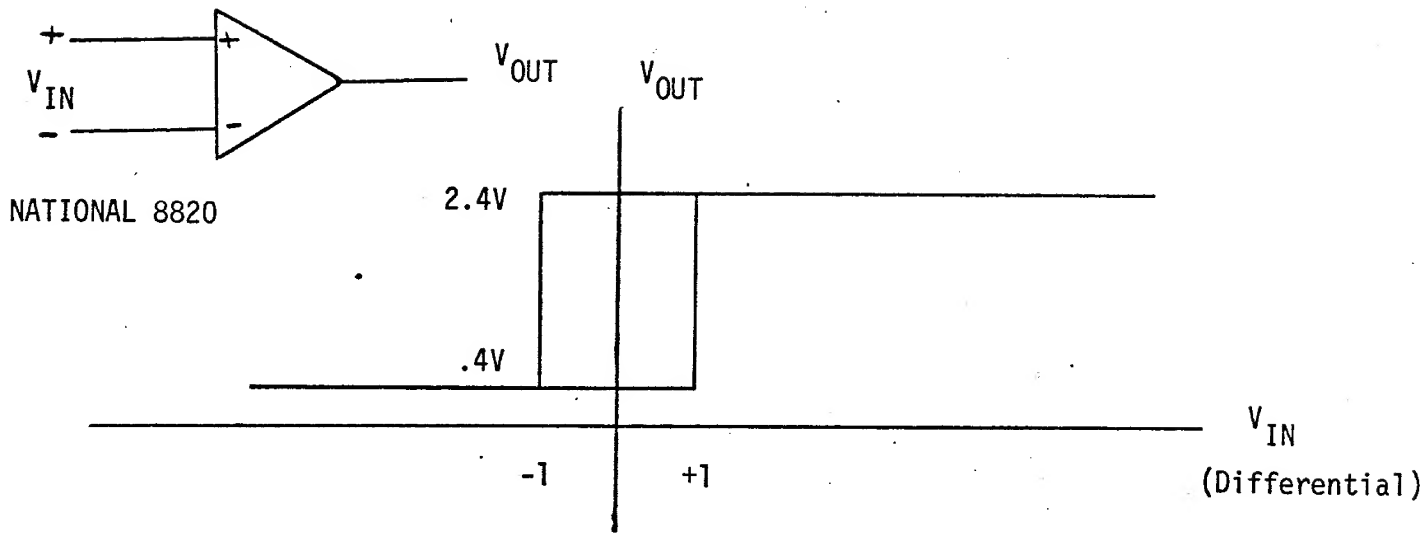
(a) Line Driver



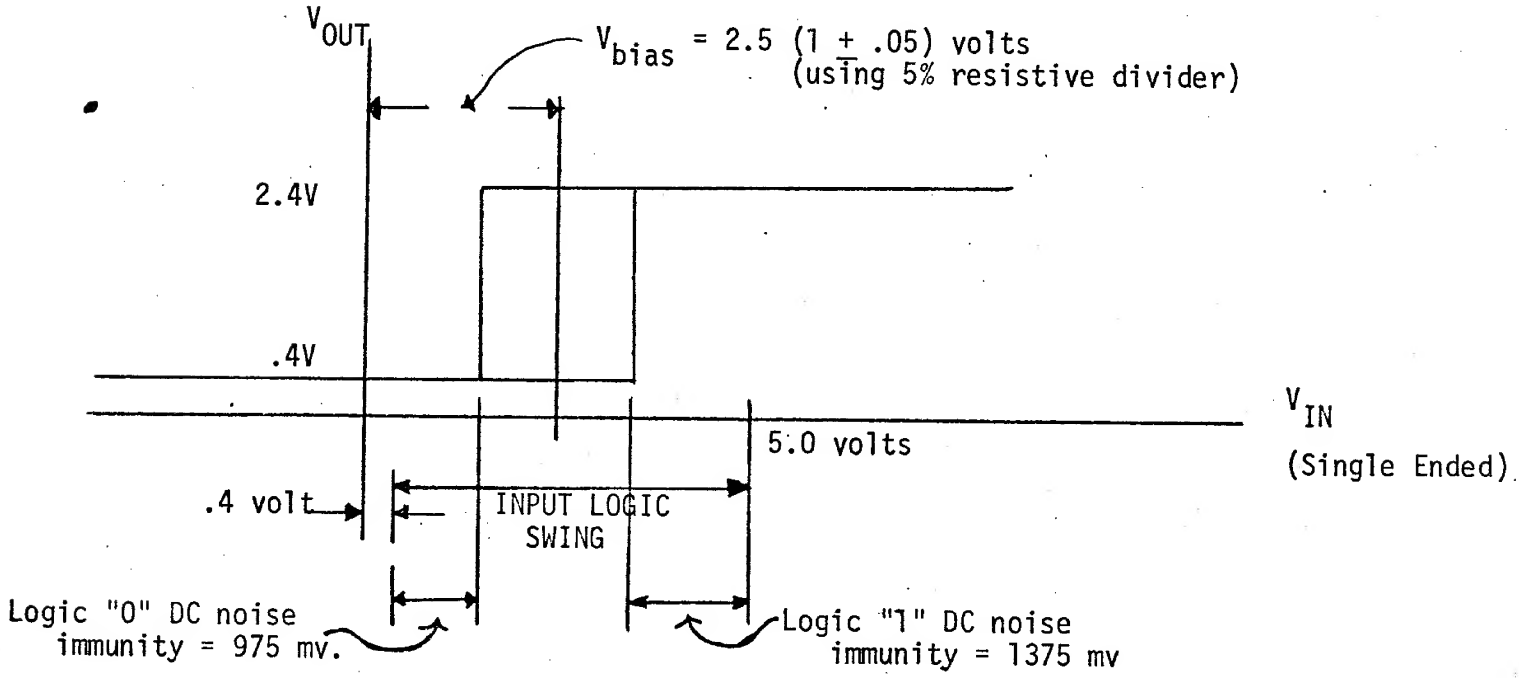
(b) Receiver Bias Network*

* Resulting Receiver Input characteristics are given in Figure 13.

Figure 12 - Positive True and Ground True TTL Configuration



(a) Receiver Transfer Function (Worst Case)



(b) Biased Receiver Transfer Function (Worst Case)

Figure 13 - Receiver Input Characteristics

I) Differential

5 volt supply - 1.787 Amps

-2 volt supply - .1 Amp

II) Positive or Negative TTL

5 volt supply - 2.151 Amps

-2 volt supply - .1 Amp

Figure 14 - I/O Power Supply Loading

Switch	Position	Function
106-S1	1	Set Flag Buffer FF on the positive edge of device flag composite.
	2	Set Flag Buffer FF on the negative edge of device flag composite.
106-S2	6	Simultaneous strobe of the input data register and setting of the Flag Buffer FF.
	5	Ungated strobing of the input data register at the trailing edge of T2.
87-S3	8	Device command FF resets on CLC.
	7	Device command FF does not reset on CLC.
97-S3	8	Device command FF resets on T2.
	0	Device command FF resets on the positive edge of device flag composite.
	9	Device command FF resets on the negative edge of device flag composite.
85-S1	1	Device command signal delayed until T5.
	2	Device command signal coincidental with device command FF.

Table 1. Lower Select Code. Control circuit function table for programmable options (refer also to Figures 2 and 9).

Switch	Position	Function
106-S3	9	Set Flag Buffer FF on the positive edge of device flag composite.
	0	Set Flag Buffer FF on the negative edge of device flag composite.
87-S1	2	Device command FF resets on CLC.
	1	Device command FF does not reset on CLC.
97-S2	6	Device command FF resets on T2.
	5	Device command FF resets on the positive edge of device flag composite.
	4	Device command FF resets on the negative edge of device flag composite.
87-S2	5	Device command' signal delayed until T5
	4	Device command' signal coincident with device command FF.
97-S1	2	HSC inhibited.
	1	HSC enabled.

Table 2. Higher Select Code. Control circuit function table for programmable options (refer also to Figures 3 and 9).

Switch	Position	Function
102-S	1	LSC device flag composite used for input register Bit 0.
	2	I/O device Bit 0 used for input register Bit 0.
85-S3	8	LSC control FF to control output line CW 10.
	9	HSC control FF to control output line CW 10.
	0	Control register Bit 10 to output line CW 10.
85-S2	5	H Dev CM D' to H Dev CMD output line.
	6	Control register Bit 10 to H Dev CMD output line.
102-S3	9	H Dev FLG + PON + L Dev FLG = L Dev FLG composite.
	0	H Dev FLG composite, L Dev FLG = L Dev FLG composite.
102-S2	6	Power on CKT enabled.
	7	Power on CKT disabled.

Table 3. Function Table for Miscellaneous Switches. (Refer to Figures 4, 5 and 9.)

HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

12930A

UNIVERSAL INTERFACE KIT

(FOR THE HP 2100 SERIES COMPUTERS)

Printed-Circuit Assemblies:
12930-60001 (Standard), Series 1214
12930-60004 (Option 001), Series 1214
12930-60005 (Option 002), Series 1214

Options Covered

This manual applies to options 001 and 002 as well as to the standard version of the HP 12930A Universal Interface Kit.

12930-90001

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

PRINTED: DEC 1972

CONTENTS

ILLUSTRATIONS

TABLES

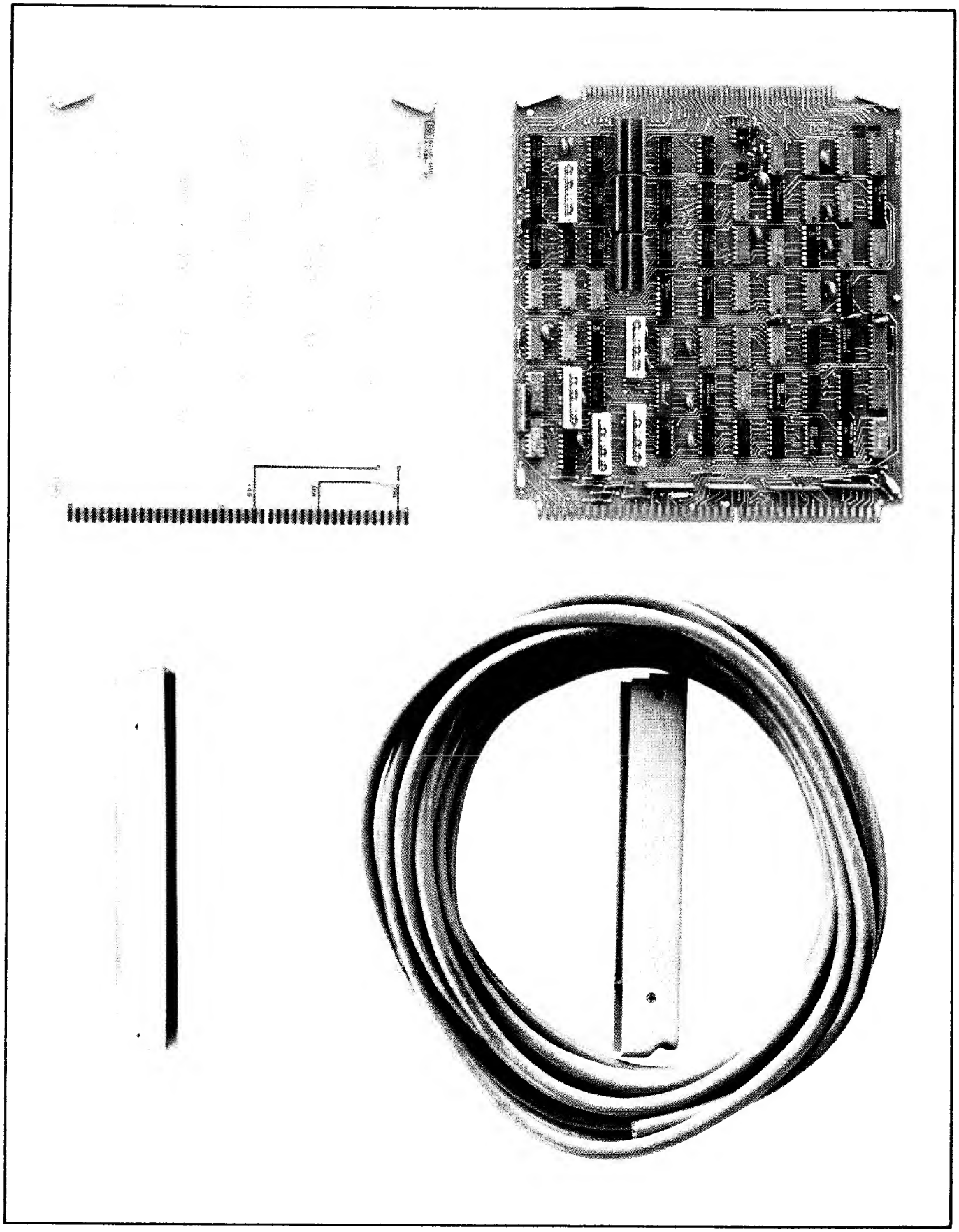


Figure 1-1. HP 12930A Universal Interface Kit

SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides general information, installation, programming, maintenance, and replaceable parts information for the HP 12930A Universal Interface Kit. (See figure 1-1.)

1-3. GENERAL DESCRIPTION.

1-4. The universal interface kit provides a means of bidirectional control and data transfer between an HP 2100 series computer and a peripheral input/output device or another computer. Logic compatibility and extended-distance transmission capability are accomplished with optional circuit configurations; the configuration of programmable switches on the printed-circuit assembly (PCA) allow the kit to interface the computer with input/output devices of varying complexity.

1-5. Logic compatibility with the interfaced device is achieved by specifying an interface kit with ground-true TTL driver (option 001), positive-true TTL driver (option 002), or differential driver (standard) input/output logic circuits.

1-6. The standard (differential driver) interface kit allows direct data transfer up to 500 feet (153 meters); the TTL-compatible interface kits allow direct data transfer up to 25 feet (7.6 meters). Maximum direct data transfer rate of 2 megabytes per second is ensured at distances up to 25 feet where controller delays are minimal.

1-7. Interfacing to devices of varying complexity is achieved by configuring programmable switches according to specific input/output device requirements. The programmable switches include a provision for selecting a second interface channel for devices requiring the exchange of command and status information in addition to normal data transfer.

1-8. The control circuits are contained on a PCA that installs in the I/O portion of the computer card cage. The cable connects the PCA to the input/output device.

1-9. INTERFACE KIT CONTENTS.

1-10. The interface kit consists of the items listed in table 1-1. The priority jumper PCA is necessary to maintain the computer interrupt priority chain when both interface PCA channels are used.

1-11. IDENTIFICATION.

1-12. PRINTED-CIRCUIT ASSEMBLY.

1-13. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked beneath the part number on the PCA. The letter identifies the revision of the etched-trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics of the loaded PCA and the positions of the components. The two-digit division code identifies the division of Hewlett-Packard that manufactured the PCA. If the series number does not correspond exactly with the series number on the title page of this manual, the PCA differs from the one described in this manual. These differences are covered in manual supplements available at the nearest HP Sales and Service Office listed at the back of this manual.

1-14. DIAGNOSTIC TEST CONNECTOR.

1-15. The hood of the diagnostic test connector is stamped "TEST CONNECTOR" together with the appropriate part number listed in table 1-1.

1-16. SPECIFICATIONS.

1-17. Specifications of the interface PCA are listed in table 1-2.

Table 1-1. Interface Kit Contents

INTERFACE KIT	PCA PART NO.	DIAGNOSTIC TEST CONNECTOR	INTERCONNECTING CABLE KIT	PRIORITY JUMPER PCA
Standard	12930-60001	12930-60006	12930-60007	02116-6110
Option 001	12930-60004	12930-60008	12930-60007	02116-6110
Option 002	12930-60005	12930-60009	12930-60007	02116-6110

Table 1-2. Specifications

Data Transfer Rate:	≤2 megabytes/second up to 25 feet (7.6 meters).
Data Transfer Distance	
Standard:	≤500 feet (153 meters).
Options 001 and 002:	≤25 feet (7.6 meters).
Number of Channels:	1 or 2, switch selectable.
I/O Logic Compatibility	
Standard:	Differential driver.
Option 001:	Ground-true TTL driver.
Option 002:	Positive-true TTL driver.
Power Requirements	
Standard:	+4.5V @ 1.8A; -2.0V @ 0.1A.
Options 001 and 002:	+4.5V @ 2.2A; -2.0V @ 0.1A.
PCA Dimensions	
Width:	7-3/4 inches (19.7 cm).
Height:	8-11/16 inches (22.1 cm).
Weight	
Net:	18 ounces (545 grams).
Shipping:	2 pounds (908 grams).

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides unpacking, initial inspection, and installation information for the HP 12930A Universal Interface Kit. The computer and input/output device should be installed and prepared for operation before installing the interface kit.

2-3. UNPACKING AND INITIAL INSPECTION.

2-4. If the interface kit is received separately from the computer, inspect the carton containing the kit before opening. If there is external evidence of damage, or if the carton rattles, request that the carrier's agent be present when the carton is opened.

2-5. Inspect each component of the kit as the parts are unpacked. If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-6. PREPARATION FOR INSTALLATION.

2-7. POWER REQUIREMENTS.

2-8. The interface PCA obtains operating power directly from the computer power supply. Before installing the interface PCA into the computer card cage, determine if the additional PCA will overload the computer power supply. (The power required by the standard and optional interface kits is specified in table 1-2.) If the addition of the interface PCA will overload the computer power supply, an appropriate computer I/O extender listed in table 2-1 must be used.

Note: If the interface kit is to be used in a system under DMA control, the interface PCA must be installed in the computer mainframe unless an I/O extender having DMA capability is available. As indicated in table 2-1, the HP 2155A is the only I/O extender currently capable of DMA operation.

2-9. CABLE FABRICATION.

2-10. To maintain the universality of the interface kit, the interconnecting cable is supplied disassembled to permit user configuration according to specific need. The cable should be fabricated as follows:

a. Insert approximately 10 inches (25 centimeters) of twisted-pair cable, part no. 8120-1895, into connector hood. (See figure 2-1.)

b. Remove approximately 5 inches (13 centimeters) of outer jacket from cable end.

c. Separate twisted-pair wires into five groups of 10 pairs each.

d. Starting at connector end nearest pins 50A and 50B, connect first group of 10 pairs as follows (record pin numbers versus wire color codes for future use):

(1) Solder the 10 multicolored wires to their respective pins on A-side of connector; eg, 50A, 49A.....41A. Insulate each pin with shrink tubing as shown in figure 2-1.

(2) Solder the white wire of each twisted-pair to the respective pins on the B-side of connector; eg, solder to pin 50B the white wire associated with multicolored wire soldered to pin 50A. Insulate each pin with shrink tubing.

e. Repeat step d with the remaining four groups of 10 twisted-pairs.

Table 2-1. Computer I/O Extenders

COMPUTER	I/O EXTENDER
HP 2100A	HP 2155A*
HP 2114A	HP 2151A
HP 2114B	HP 2151A
HP 2115A	HP 2150B
HP 2116A	HP 2150A
HP 2116B	HP 2150B
HP 2116C	HP 2150B

*Includes DMA capability.

f. Assemble connector and hood as shown in figure 2-1.

g. Attach appropriate I/O device connector to unterminated end of cable; use pin numbers versus wire color codes recorded previously and the interface connector pin assignments given in table 2-2 to prepare I/O device connector.

2-11. PROGRAMMABLE SWITCH SETTINGS.

2-12. To maintain the universality of the interface kit, programmable switches are provided to permit configuration of various interface circuits according to specific requirements. The programmable switches are set using a screwdriver to position the contact mechanism. Set the programmable switches as required according to the switch setting function definitions given in tables 2-3, 2-4, and 2-5.

2-13. TRANSFER RATE CONSIDERATIONS.

2-14. When the system in which the universal interface is used is operating in the DMA mode, the universal interface can accommodate data transfer rates up to 2 million bytes per second over distances up to 25 feet (7.6 meters). High data transfer rates are achieved by effecting successive DMA cycle steals; ie, the DMA channel receives a Flag signal to request more data before the CPU timing has advanced past the period when a new DMA cycle can begin. The time delay between the issuance of the Device Command and the receipt of the Flag signal by the CPU is critical to effect successive cycle steals. The maximum delay that can be introduced by the I/O device controller and interface cable, and still effect successive cycle steals, is given by

$$d_{max(ns)} = 102 - 3\ell$$

where

d = introduced delay and
ℓ = length of interface cable in feet, assuming 1.5 ns per foot transmission line delay.

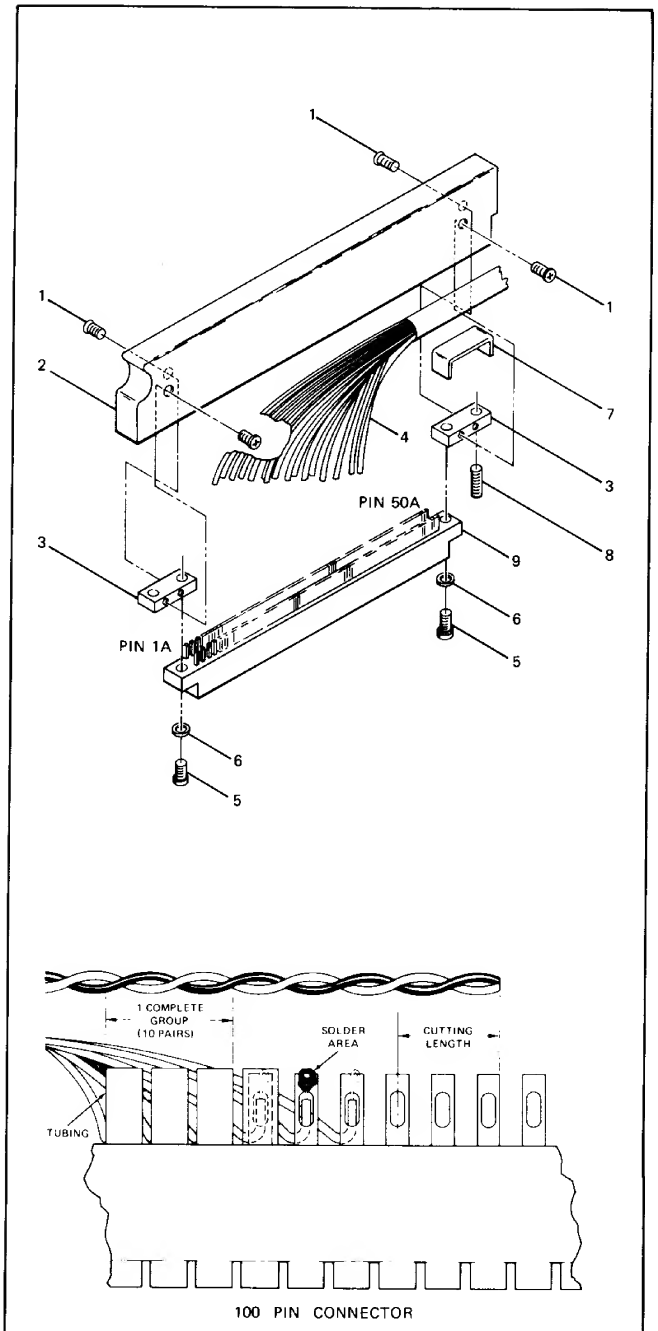
Note: To achieve maximum data transfer rate, capacitors C43 and C45 must be removed from the universal interface PCA.

2-15. INSTALLATION.

2-16. Install the interface PCA in the computer mainframe as follows:

a. Set computer and input/output device POWER switches to OFF.

b. Open computer for access to I/O card cage and install interface PCA into the slot corresponding to desired I/O select code for interface channel. (If the programmable switches are set to enable the second interface channel, the I/O slot used will determine the select code of the higher priority "data" channel.)



ITEM	DESCRIPTION	PART NO.
1	Screw, flathead 4-40, 0.375	2200-0144
2	Hood	5020-7329
3	Mounting block connector	5020-7319
4	Cable, 50 twisted pair	8120-1895
5	Screw, external locking	2200-0111
6	Washer, flat	3050-0229
7	Cable clamp	5000-8038
8	Set screw; 4-40, 0.5	3030-0144
9	Connector, 100 pin	1251-2658

2235-2

Figure 2-1. Cable Fabrication Diagram and Parts List

Table 2-2. Interface Connector (J1) Pin Assignments

J1 PIN	SIGNAL	J1 PIN	SIGNAL
1A	BO 15	26A	Bit 15
1B	"Not" BO 15	26B	"Not" Bit 15
2A	BO 14	27A	Bit 14
2B	"Not" BO 14	27B	"Not" Bit 14
3A	BO 13	28A	Bit 13
3B	"Not" BO 13	28B	"Not" Bit 13
4A	BO 12	29A	Bit 12
4B	"Not" BO 12	29B	"Not" Bit 12
5A	BO 11	30A	Bit 11
5B	"Not" BO 11	30B	"Not" Bit 11
6A	BO 10	31A	Bit 10
6B	"Not" BO 10	31B	"Not" Bit 10
7A	BO 9	32A	Bit 9
7B	"Not" BO 9	32B	"Not" Bit 9
8A	BO 8	33A	Bit 8
8B	"Not" BO 8	33B	"Not" Bit 8
9A	BO 7	34A	Bit 7
9B	"Not" BO 7	34B	"Not" Bit 7
10A	BO 6	35A	Bit 6
10B	"Not" BO 6	35B	"Not" Bit 6
11A	BO 5	36A	Bit 5
11B	"Not" BO 5	36B	"Not" Bit 5
12A	BO 4	37A	Bit 4
12B	"Not" BO 4	37B	"Not" Bit 4
13A	BO 3	38A	Bit 3
13B	"Not" BO 3	38B	"Not" Bit 3
14A	BO 2	39A	Bit 2
14B	"Not" BO 2	39B	"Not" Bit 2
15A	BO 1	40A	Bit 1
15B	"Not" BO 1	40B	"Not" Bit 1
16A	BO 0	41A	Bit 0
16B	"Not" BO 0	41B	"Not" Bit 0
17A	CW 15	42A	STS 6
17B	"Not" CW 15	42B	"Not" STS 6
18A	CW 14	43A	STS 5
18B	"Not" CW 14	43B	"Not" STS 5
19A	CW 13	44A	STS 4
19B	"Not" CW 13	44B	"Not" STS 4
20A	CW 12	45A	STS 3
20B	"Not" CW 12	45B	"Not" STS 3
21A	CW 11	46A	STS 2
21B	"Not" CW 11	46B	"Not" STS 2
22A	CW 10	47A	STS 1
22B	"Not" CW 10	47B	"Not" STS 1
23A	Command Channel Device Command	48A	"Not" Command Channel Device Flag
23B	"Not" Command Channel Device Command	48B	Command Channel Device Flag
24A	Data Channel Device Command	49A	Data Channel Device Flag
24B	"Not" Data Channel Device Command	49B	"Not" Data Channel Device Flag
25A	Power On Normal (PON) Out	50A	Signal Ground
25B	Power On Normal (PON) In	50B	Signal Ground

Notes:

BO 15:0 = Data output to device.
CW 15:10 = Command word output to device.
Bits 15:0 = Data input from device.
STS 6:1 = Status input from device.

Table 2-3. Programmable Switch Settings for High Priority Interface Channel

PROGRAMMABLE SWITCH	POSITION	FUNCTION
U106S1	1	Set Data Channel Flag Buffer FF on positive-going edge of Data Channel Device Flag composite.
	2	Set Data Channel Flag Buffer FF on negative-going edge of Data Channel Device Flag composite.
U106S2	5	Ungated strobe of input data register at trailing edge of T2 pulse from computer.
	6	Simultaneous strobe of input data register and setting of Data Channel Flag Buffer FF.
U87S3	7	Data Channel Command FF does not clear on CLC instruction from computer.
	8	Data Channel Command FF cleared by CLC instruction from computer.
U97S3	8	Data Channel Command FF cleared by T2 pulse from computer.
	9	Data Channel Command FF cleared on negative-going edge of Data Channel Device Flag composite.
	0	Data Channel Command FF cleared on positive-going edge of Data Channel Device Flag composite.
U85S1	1	Data Channel Device Command signal delayed until T5.
	2	Data Channel Device Command signal issued coincidental with setting of Data Channel Command FF.

c. If interface PCA is to be used in the two-channel mode, the priority jumper PCA, part no. 02116-6110, must be installed in next lower priority I/O slot to maintain proper operation of interrupt priority chain.

d. Route interconnecting cable into computer and attach 100-pin connector to J1 of interface PCA.

e. Connect interconnecting cable to input/output device as required and set computer and input/output device POWER switches to ON.

f. Verify proper operation by performing the HP 12930A Universal Interface Test, part no. 12930-90004, contained in the *Manual of Diagnostics.*

2-17. RESHIPMENT.

2-18. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the number of the kit.

2-19. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-20. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "Fragile" to ensure careful handling.

Note: In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

Table 2-4. Programmable Switch Settings for Low Priority Interface Channel

PROGRAMMABLE SWITCH	POSITION	FUNCTION
U97S1	1	Command channel enabled.
	2	Command channel inhibited.
U106S3	9	Set Command Channel Flag Buffer FF on positive-going edge of Command Channel Device Flag composite.
	0	Set Command Channel Flag Buffer FF on negative-going edge of Command Channel Device Flag composite.
U87S1	1	Command Channel Command FF does not clear on CLC instruction from computer.
	2	Command Channel Command FF cleared by CLC instruction from computer.
U97S2	4	Command Channel Command FF cleared on negative-going edge of Command Channel Device Flag composite.
	5	Command Channel Command FF cleared on positive-going edge of Command Channel Device Flag composite.
	6	Command Channel Command FF cleared by T2 pulse from computer.
U87S2	4	Command Channel Device Command signal issued coincidental with setting of Command Channel Command FF.
	5	Command Channel Device Command signal delayed until T5.

Table 2-5. Programmable Switch Settings for General Purpose Functions

PROGRAMMABLE SWITCH	POSITION	FUNCTION
U102S1	1	Data Channel Device Flag composite used for input data register bit 0.
	2	Input/output device bit 0 used for input data register bit 0.
U85S3	8	Data Channel Control signal to control command word bit 10 (CW 10).
	9	Command Channel Control signal to control command word bit 10 (CW 10).
	0	Output control register bit 10 to control command word bit 10 (CW 10).
U85S2	5	Command Channel Device Command signal connected to Command Channel Device Command output.
	6	Output control register bit 10 connected to Command Channel Device Command output.
U102S3	9	Command Channel Device Flag + PON + Data Channel Device Flag = Data Channel Device Flag composite.
	0	Command Channel Device Flag + PON = Command Channel Device Flag composite.
U102S2	6	Power-on-normal (PON) circuit enabled.
	7	Power-on-normal (PON) circuit disabled.

SECTION III PROGRAMMING

3-1. INTRODUCTION.

3-2. This section contains programming considerations for systems employing the HP 12930A Universal Interface Kit. Included are typical assembly language programs that transfer data to and from the interface.

3-3. INPUT/OUTPUT DEVICE CHARACTERISTICS.

3-4. The interface kit will interface an HP 2100 series computer to a wide variety of input/output devices and to other computers. The interface can operate in systems with or without DMA capability and can interface devices with the following characteristics:

a. Requires interface with one or two interface channels.

b. Capable of data transfer rates $\leqslant$2 megabytes per second over distances up to 25 feet (7.6 meters).

c. Requires either positive-true TTL, ground-true TTL, or differential driver input/output logic compatibility.

d. If two interface channels required, will issue $\leqslant$ six command bits.

e. If two interface channels required, will recognize $\leqslant$ six status bits.

3-5. PROGRAMMING CONSIDERATIONS.

3-6. Data is transferred between the computer and interface by an OTA/B or LIA/B instruction addressed to the interface channel. Commands are transferred to the interface by an OTA/B instruction addressed to the interface command channel; status is transferred from the interface by an LIA/B instruction addressed to the interface command channel. Table 3-1 lists command word bit assignments used by the interface; table 3-2 lists the status word bit assignments recognized by the interface.

Note: If the interface is in the single-channel mode, the interface channel address will correspond to the PCA position number in the I/O card cage. If the interface is in the two-channel mode, the PCA position number will correspond to the higher priority "data" channel. The address of the lower priority "command" channel will correspond to the data channel address plus 1 (octal).

Table 3-1. Command Word Bit Assignments

BIT	FUNCTION
0 through 9	Not used
10	(Command register bit 10 • U85S2 position 6) + (Command Channel Device Command • U85S2 position 5)
11	Command register bit 11 + CRS Stretched
12	Command register bit 12
13	Command register bit 13
14	Command register bit 14
15	Command register bit 15

Table 3-2. Status Word Bit Assignments

BIT	FUNCTION
0	Command Channel Flag FF
1	User-defined status bit 1
2	User-defined status bit 2
3	User-defined status bit 3
4	User-defined status bit 4
5	User-defined status bit 5
6	User-defined status bit 6
7	Power-on-normal (PON) status
8	CRS Stretched
9	Command Channel Command Signal
10	Command word bit 10
11	Command word bit 11
12	Command word bit 12
13	Command word bit 13
14	Command word bit 14
15	Command word bit 15

3-7. Data is transferred between the interface and input/output device according to the state of the Flag FF on the interface PCA. The Flag FF is controlled by signals from the input/output device to indicate the readiness of the device to receive or send data.

3-8. When interfacing an input-only device, a set Flag FF will indicate data is present in the interface input register and ready for transfer to the computer. A clear Flag FF will indicate the device is transferring data to the interface.

3-9. When interfacing an output-only device, a set Flag FF will indicate the device has accepted previous data (if applicable) and is ready to receive more data. A clear Flag FF signal will indicate the device will not accept more data.

3-10. When interfacing an input/output device, data transfer operations using both registers can be performed simultaneously but the Flag FF state can be associated with only one register at a time. During a data input operation, a set Flag FF will indicate data is present in the interface input register and ready for transfer to the computer. A program instruction to clear the Flag FF (STC,C) must be issued before the data output operation. During the subsequent output operation, the set Flag FF will indicate the device has accepted the previous data and is ready to receive more data.

3-11. Table 3-3 is a sample program for transferring data to and from the interface using the "skip-flag" technique and table 3-4 is a sample program for transferring data under DMA control. The object of the sample DMA program is to input a block of 50 words and store the information in memory starting at address 200_8. The sample program assumes use of DMA channel 1 and the input device has select code 10_8. The program could be changed to operate on DMA channel 2 by changing the DMA channel select codes from 2 to 3 and from 6 to 7.

Table 3-3. Sample Assembly Language Program Using "Skip-Flag" Technique

LABEL	OPCODE	OPERAND	COMMENTS
DEF		XXB	Device select code (octal).
INPUT	NOP		Entry point.
	STC	XXB,C	Start I/O device.
	SFS	XXB	Operation completed?
	JMP	*-1	No, wait.
	LIA	XXB	Load input data into A-register.
	JMP	INPUT,I	Return to main program.
OUTPT	NOP		Entry point.
	SFS	XXB	Device ready for data?
	JMP	*-1	No, wait.
	OTA	XXB	Output data to device interface.
	STC	XXB,C	Execute transfer to I/O device.
	JMP	OUTPUT,I	Return to main program.

Table 3-4. Sample Assembly Language Program to Transfer Data Under DMA Control

LABEL	OPCODE	OPERAND	COMMENTS
ASGN1	LDA	CW1	Fetches control word 1 (CW1) from memory and loads it in A-register.
	OTA	6	Outputs CW1 to DMA channel 1.
MAR1	CLC	2	Prepares memory address register to receive control word 2 (CW2).
	LDA	CW2	Fetches CW2 from memory and loads it in A-register.
	OTA	2	Outputs CW2 to DMA channel 1.
WCR1	STC	2	Prepares word count register to receive control word 3 (CW3).
	LDA	CW3	Fetches CW3 from memory and loads it in A-register.
	OTA	2	Outputs CW3 to DMA channel 1.
STRT1	STC	10B,C	Start input device.
	STC	6B,C	Activate DMA channel 1.
	SFS	6	Wait while data transfer takes place or, if interrupt processing is used,
	JMP	*-1	continue program.
	.		
	.		
	.		
	HLT		Halt.
CW1	OCT	120010	Assignment for DMA channel 1 (ASGN1); specifies I/O channel select code address (10_8), STC after each word is transferred, and CLC after final word is transferred.
CW2	OCT	100200	Memory address register control. DMA channel 1 (MAR1); specifies memory input operation and starting memory address (200_8).
CW3	DEC	-50	Word count register control. DMA channel 1 (WCR1); specifies the 2's complement of the number of character words in the block of data to be transferred (50_{10}).

SECTION IV THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section describes the theory of operation of the HP 12930A Universal Interface Kit.

4-3. FUNCTIONAL DESCRIPTION.

4-4. As shown in figure 4-1, the interface PCA provides one or two interface channels, as desired, for data transfer operations between an input/output device and a central processor unit (CPU). The device can be another computer that acts as an input/output device for the CPU. The higher priority "data" channel transfers 16-bit data words between the input/output device and CPU. The lower priority switch-selectable "command" channel transfers command and status information ($\leq$ six bits) between the input/output device and CPU.

4-5. The data channel includes data transfer control circuits and two storage registers. The storage registers momentarily store data bytes being transferred: one register is used for data being sent by the CPU to the input/output device and the second register is used for data being sent by the input/output device to the CPU. This momentary storage allows the interface to accept and send data when convenient for the respective devices.

4-6. Data transfer control circuits include a circuit to enable the input/output device when commanded by the CPU, a circuit to detect the signal from the input/output device that indicates a completed operation, and a circuit to signal the CPU when the input/output device requests service.

4-7. The command channel includes command control circuits and a command register. The command register stores up to six command bits sent by the CPU to the input/output device. Input/output device status ($\leq$ six bits) is strobed directly to the CPU without being stored; therefore, device status must be continuously available to the interface. The command control circuits include a circuit to enable the input/output device when commanded by the CPU, and a circuit to signal the CPU when the input/output device requests service.

4-8. DETAILED CIRCUIT DESCRIPTIONS.

4-9. DATA CHANNEL LOGIC CIRCUITS.

4-10. DATA CONTROL CIRCUITS. The Data Channel Flag Buffer FF will be set to indicate to the CPU that the input/output device requires servicing. The Flag Buffer FF can be set by a Set Flag (STF) command issued by the CPU or by a POPIO signal generated by the CPU during power turn-on and preset operations. The Flag Buffer FF can also be set by either the leading or trailing edge of a Flag signal from the input/output device as selected by programmable switch U106S1. A flowchart of the data channel operating sequence is given in figure 4-2.

4-11. The Data Channel Flag Buffer FF can be cleared by a Clear Flag (CLF) command or by an Interrupt Acknowledge (IAK) signal from the CPU. The CLF command is used to clear the Flag Buffer FF during data transfer operations to indicate the data channel is busy. The IAK signal will be issued by the CPU to indicate that a service request has been acknowledged.

4-12. The Data Channel Control FF must be set to enable data transfer operations to or from the input/output device, or to enable interrupt requests to the CPU. Both the Control and Command FF's will be set by a Set Control (STC) command addressed to the data channel. The Data Channel Control FF can be cleared to inhibit data transfer and interrupt requests by either a Control Reset (CRS) or Clear Control (CLC) command from the CPU. The Data Channel Command FF can be cleared by either a Control Reset (CRS) command or by any of the following three switch-selectable alternatives: (1) a Clear Control (CLC) command, (2) the leading or trailing edge of a Flag signal from the input/output device, or (3) by a T2 pulse from the CPU.

4-13. DATA TRANSFER CIRCUITS. Data is transferred from the CPU and loaded into the interface output data register by an OTA/B instruction addressed to the data channel. The OTA/B instruction generates the IOO signal that serves as the Output Strobe signal. Once loaded into the register, the data is presented continuously to the input/output device.

4-14. Data is transferred from the input/output device and loaded into the interface input data register by an Input Strobe signal generated by any of three switch-selectable alternatives: (1) by the T2 pulse generated by the CPU, (2) the leading edge of a Flag signal from the input/output device, or (3) the trailing edge of a Flag signal. Data is gated into the CPU by an LIA/B instruction addressed to the data channel. The LIA/B instruction generates the IOI signal that serves as the gating signal.

4-15. COMMAND CHANNEL LOGIC CIRCUITS.

4-16. The Command Channel Flag Buffer FF will be set to indicate to the CPU that the input/output device is ready

to receive a command, has completed an operation, or is requesting service. The Command Channel Control FF must be set by CPU instruction to enable the Flag signal to the CPU, and is used to enable the input/output device to execute the command contained in the interface command register. A flowchart of the command channel operating sequence is given in figure 4-3.

4-17. The Command Channel Flag Buffer FF can be set by a Set Flag (STF) command issued by the CPU or by a POPIO signal generated by the CPU at power turn-on and preset operations. The Flag Buffer FF can also be set by either the leading or trailing edge of a Flag signal from the input/output device as selected by programmable switch U106S3. Both the Command Channel Control and Command FF's will be set by a Set Control (STC) instruction addressed to the command channel. The Command Channel Control FF can be cleared to inhibit Flag signals to the CPU and to terminate input/output device operations by either a Control Reset (CRS) or Clear Control (CLC) command from the CPU. The Control Channel Command FF can be cleared by either a Control Reset (CRS) command or by any of the following three switch-selectable alternatives: (1) a Clear Control (CLC) command, (2) the leading or trailing edge of a Flag signal from the input/output device, or (3) by a T2 pulse from the CPU.

4-18. SKIP FLAG TEST CIRCUIT.

4-19. The CPU can test the interface Flag FF conditions by issuing a Skip [if] Flag Set (SFS) or Skip [if] Flag Cleared (SFC) to either interface channel. The SFS or SFC signals will be "anded" with the select code signals and Flag FF signals for both channels in the skip flag test circuit and a Skip [on] Flag (SKF) signal will be generated when the Flag FF condition corresponds to the test signal issued.

4-20. SYSTEM POWER FAULT DETECT CIRCUIT.

4-21. The system power fault detect circuit monitors the power-on status of both the input/output device and the CPU. The Power-On-Normal (PON) signal from the CPU and a power-on current sample from the input/output device are monitored simultaneously. If either the PON signal or I/O device current sample indicates a power failure, a System Power Fault signal is generated. The System Power Fault signal will be loaded into the status word and to either of the following switch-selectable alternatives: (1) the data channel control circuits to generate an interrupt request or (2) the bit 0 position of the interface input data register and the command channel control circuits to generate an interrupt request. The system power fault circuit can be disabled by programmable switch U102S2 if power fault detection is not desired.

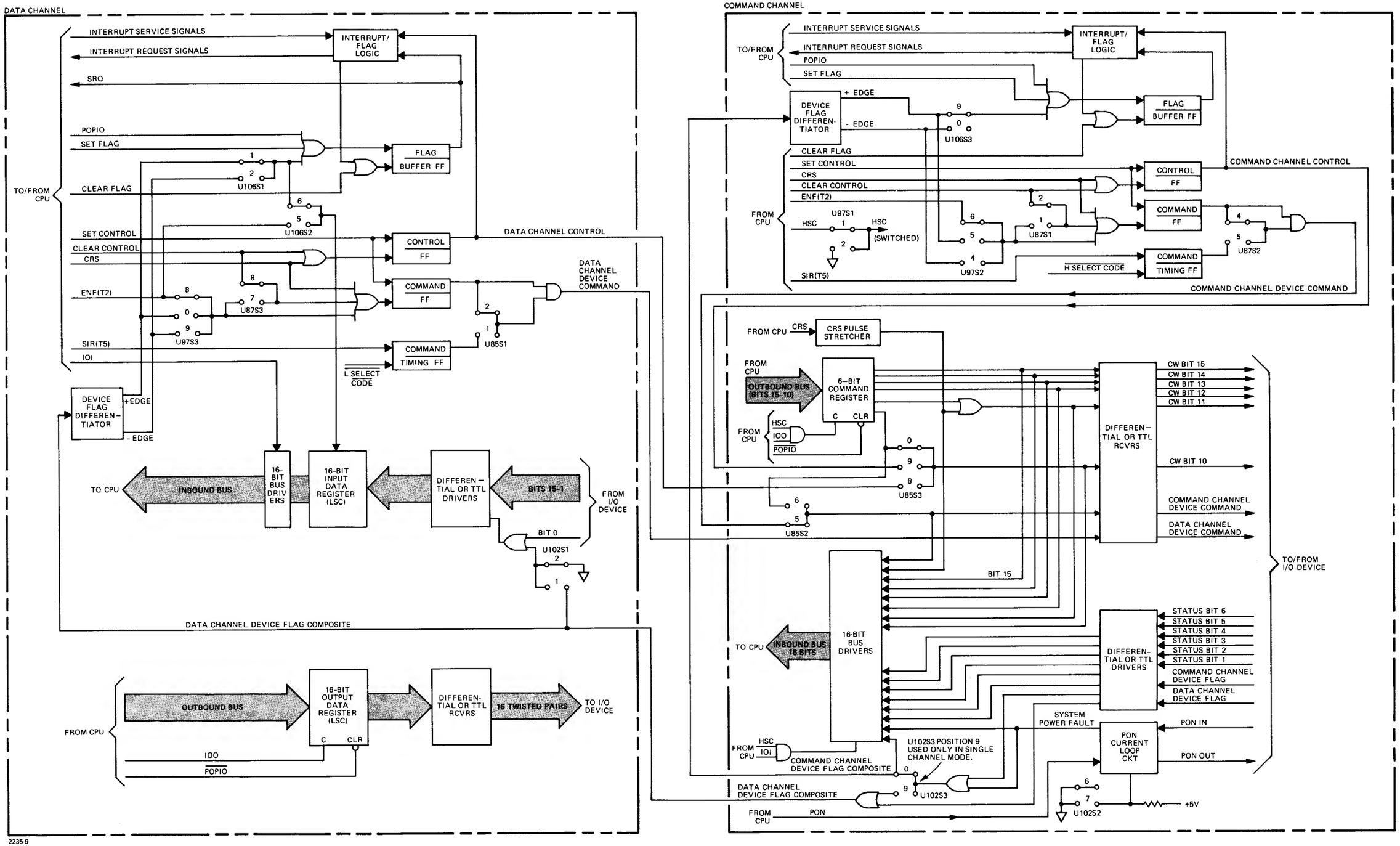


Figure 4-1. Universal Interface PCA Block Diagram

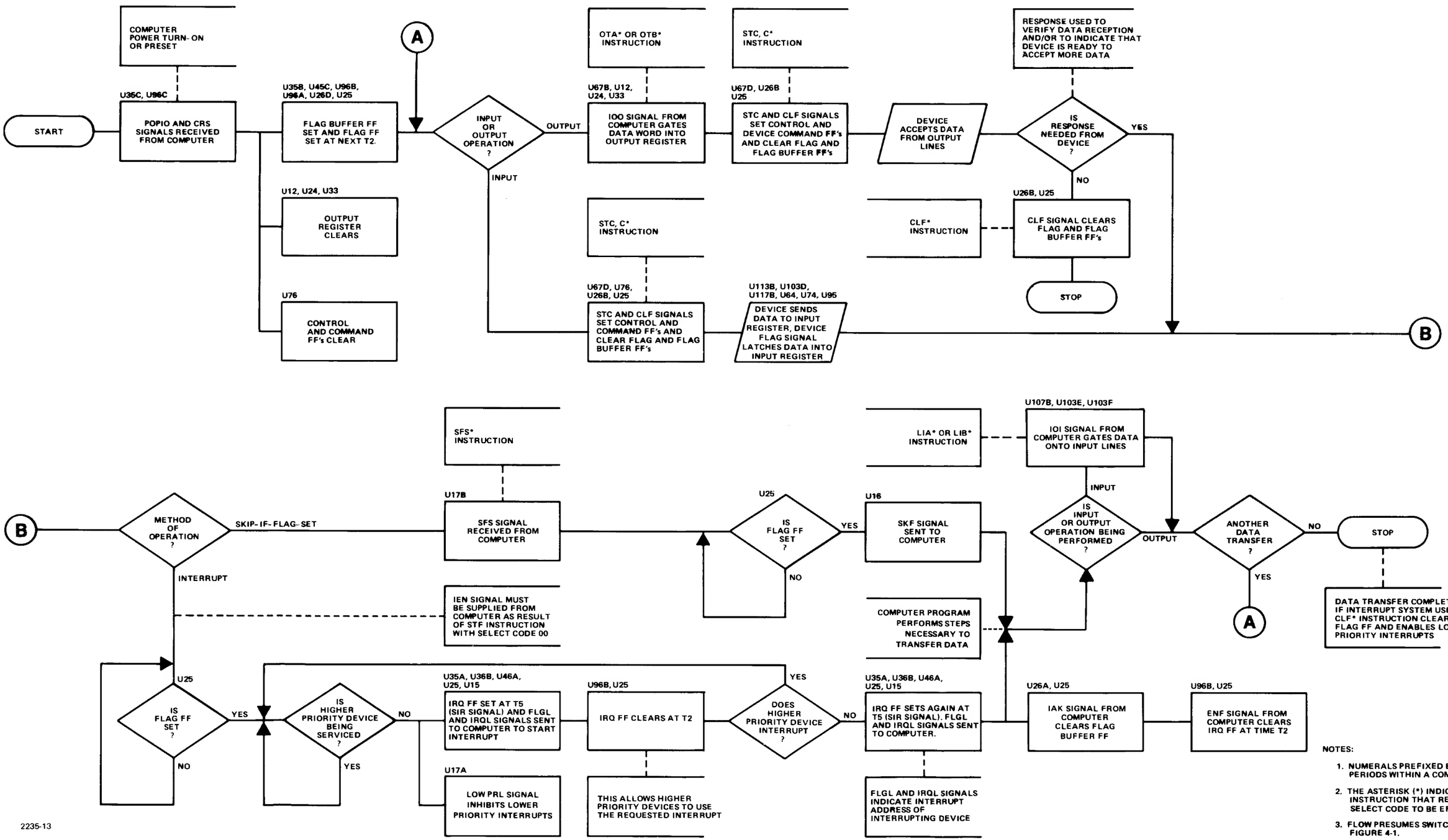
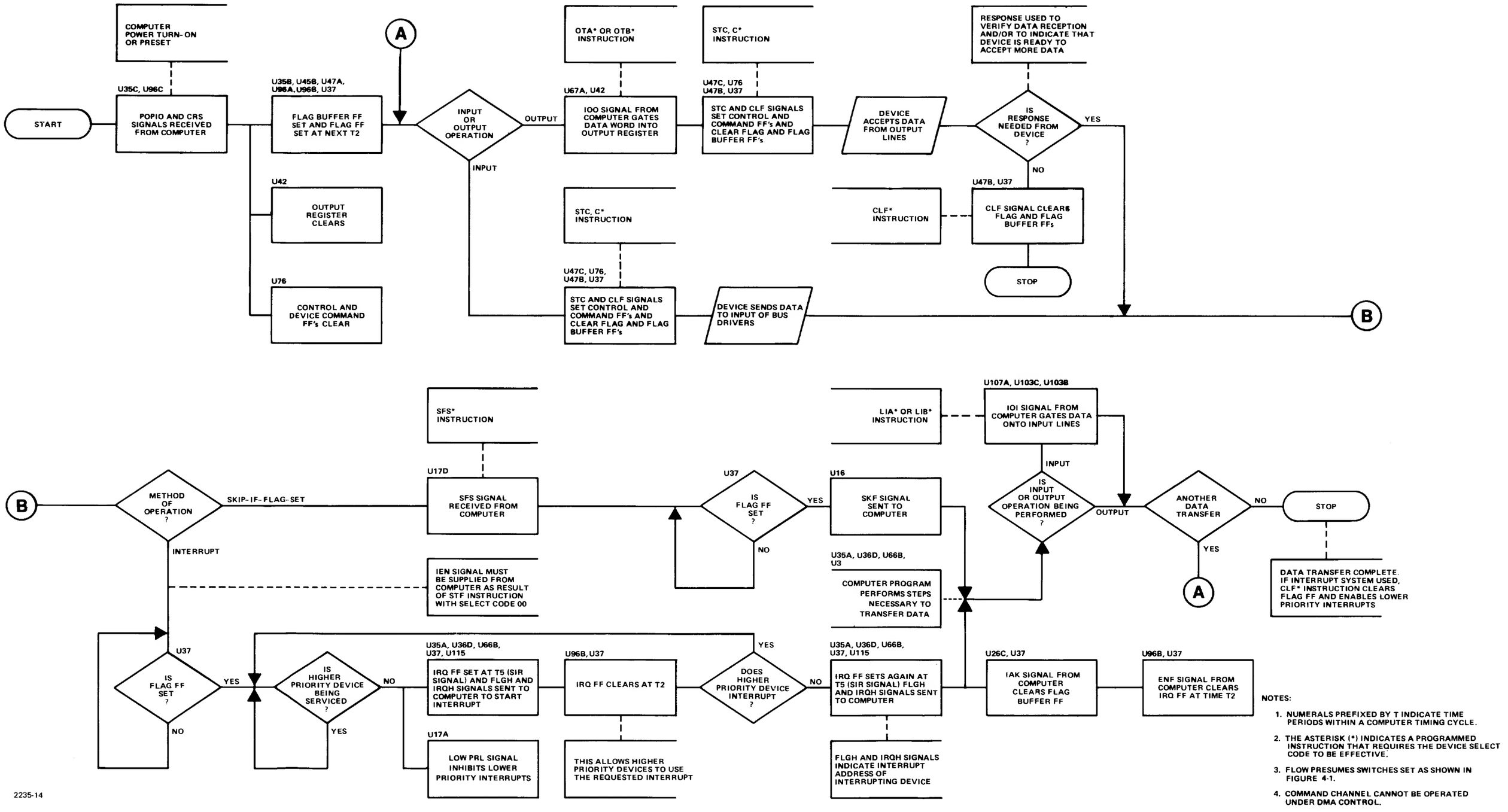


Figure 4-2. Data Channel Operating Sequence Flowchart



NOTES:

1. NUMERALS PREFIXED BY T INDICATE TIME PERIODS WITHIN A COMPUTER TIMING CYCLE.
2. THE ASTERISK (*) INDICATES A PROGRAMMED INSTRUCTION THAT REQUIRES THE DEVICE SELECT CODE TO BE EFFECTIVE.
3. FLOW PRESUMES SWITCHES SET AS SHOWN IN FIGURE 4-1.
4. COMMAND CHANNEL CANNOT BE OPERATED UNDER DMA CONTROL.

Figure 4-3. Command Channel Operating Sequence Flowchart

SECTION V MAINTENANCE

5-1. INTRODUCTION.

5-2. This section provides maintenance information for the HP 12930A Universal Interface Kit. Included are preventive maintenance and troubleshooting instructions, parts location views, schematic diagrams, and integrated circuit details.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are provided in the computer documentation. There are no separate preventive maintenance procedures to be performed on the interface PCA.

5-5. DIAGNOSTICS.

5-6. Procedures for running the appropriate diagnostic are contained in the HP 12930A Universal Interface Test, part no. 12930-90004, contained in the *Manual of Diagnostics.* Wire lists of the diagnostic test connectors are given in tables 5-1 through 5-3.

5-7. TROUBLESHOOTING.

5-8. Troubleshooting the interface kit is accomplished by performing the universal interface test and analyzing the error halts that occur as the test is being run. To further isolate a malfunction, refer to integrated circuit, parts location, and schematic diagrams in figures 5-1 through 5-5. Tables 5-4 through 5-6 list replaceable parts for the standard and optional PCA's.

Table 5-1. Diagnostic Test Connector (12930-60008) Wire List

FROM PIN	TO PIN	FROM PIN	TO PIN
B1	B26	B14	B39
B2	B27	B15	B40
B3	B28	B16	B41
B4	B29	B17	B42
B5	B30	B18	B43
B6	B31	B19	B44
B7	B32	B20	B45
B8	B33	B21	B46
B9	B34	B22	B47
B10	B35	B23	B48
B11	B36	B24	B49
B12	B37	B25	B50
B13	B38		

Table 5-2. Diagnostic Test Connector (12930-60006) Wire List

FROM PIN	TO PIN	FROM PIN	TO PIN
A1	A26	B1	B26
A2	A27	B2	B27
A3	A28	B3	B28
A4	A29	B4	B29
A5	A30	B5	B30
A6	A31	B6	B31
A7	A32	B7	B32
A8	A33	B8	B33
A9	A34	B9	B34
A10	A35	B10	B35
A11	A36	B11	B36
A12	A37	B12	B37
A13	A38	B13	B38
A14	A39	B14	B39
A15	A40	B15	B40
A16	A41	B16	B41
A17	A42	B17	B42
A18	A43	B18	B43
A19	A44	B19	B44
A20	A45	B20	B45
A21	A46	B21	B46
A22	A47	B22	B47
A23	A48	B23	B48
A24	A49	B24	B49
A25	A50	B25	B50

Table 5-3. Diagnostic Test Connector (12930-60009) Wire List

FROM PIN	TO PIN	FROM PIN	TO PIN
A1	A26	A14	A39
A2	A27	A15	A40
A3	A28	A16	A41
A4	A29	A17	A42
A5	A30	A18	A43
A6	A31	A19	A44
A7	A32	A20	A45
A8	A33	A21	A46
A9	A34	A22	A47
A10	A35	A23	A48
A11	A36	A24	A49
A12	A37	A25	A50
A13	A38		

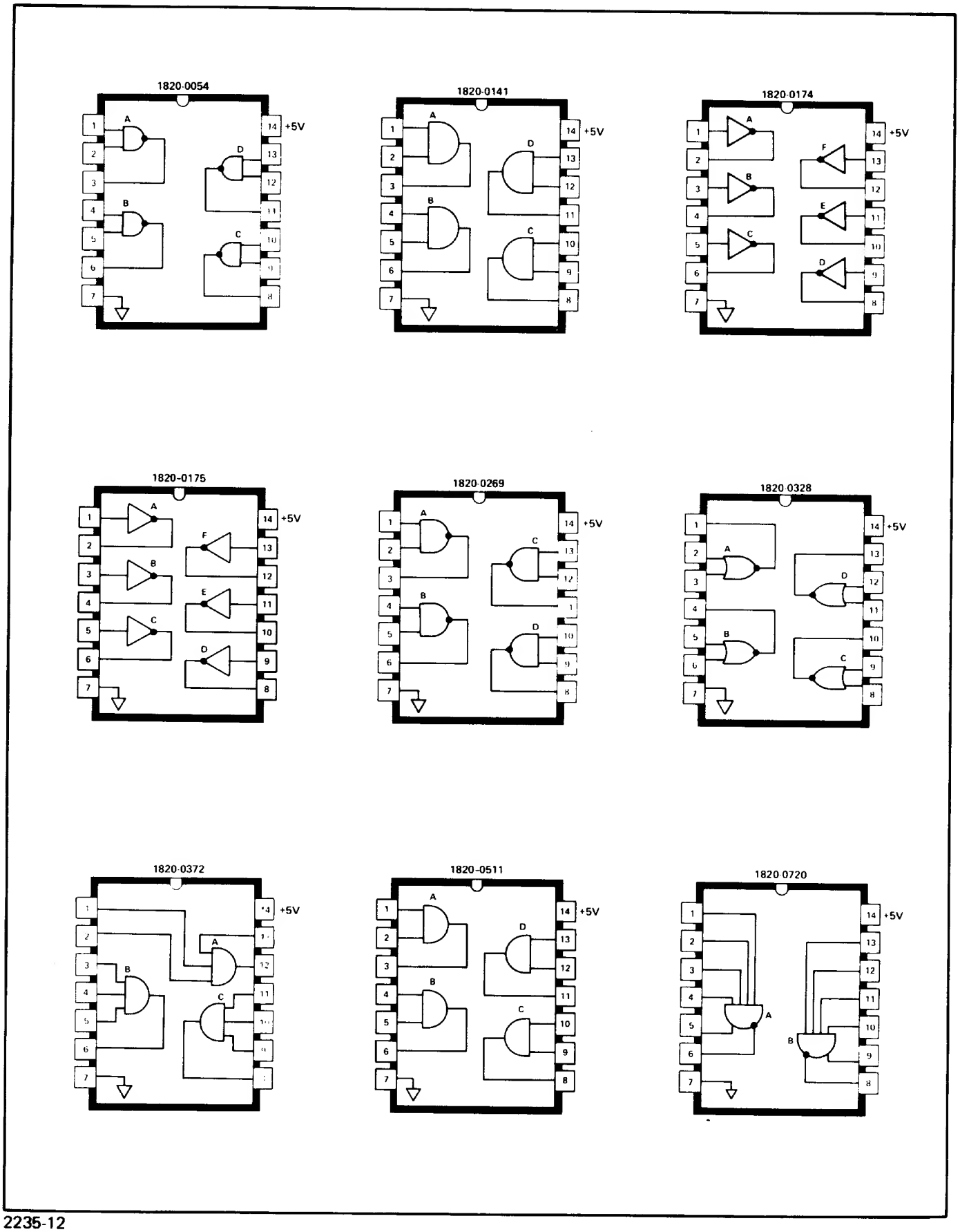
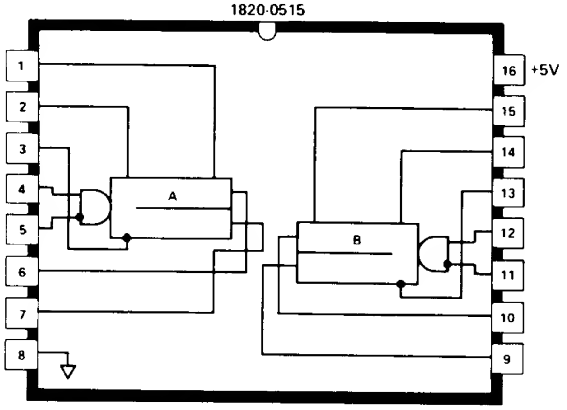
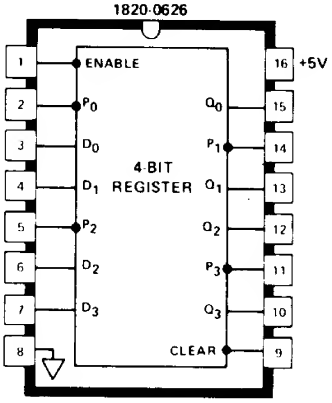


Figure 5-1. Integrated Circuit Diagrams (Sheet 1 of 2)

1820-0515

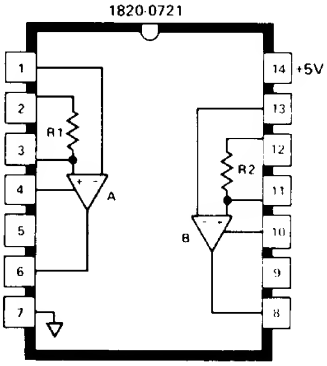


1820-0626



A low input on the ENABLE line allows data on the input lines to set the register. There are two modes of operation, one using the D input lines (most common) and the other using P input lines.

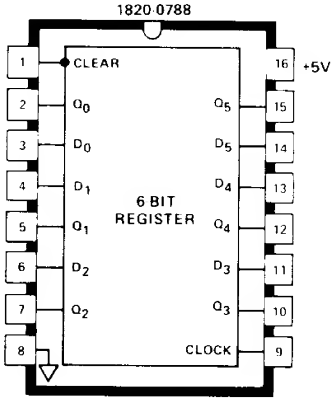
1820-0721



If the D inputs are used the P inputs are held false. When the ENABLE line is low the register output lines will "follow" the D inputs. When the ENABLE line goes high the register will retain the last set of data inputs.

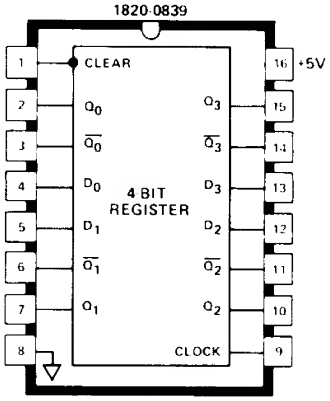
If the P inputs are used the D inputs are held true. When the ENABLE line is low, a false input on the P line will set the register bit. The register is then cleared by a low signal on the CLEAR line. The CLEAR line serves as a "master" register clear for both the D and P modes of operation.

1820-0788



Data on the input lines is entered into the register by a positive-going transition of the CLOCK line. The register is cleared by a low input on the CLEAR line.

1820-0839



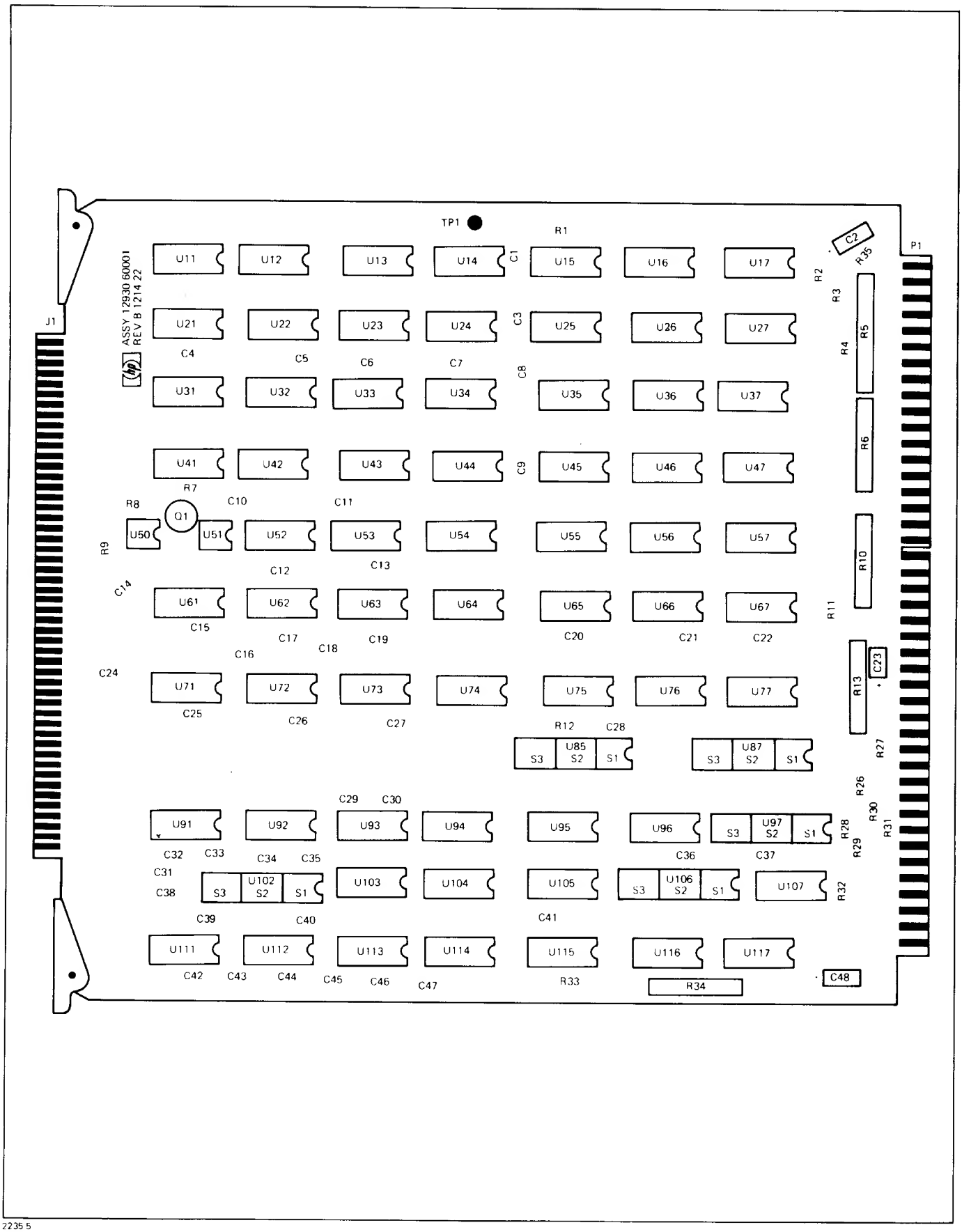
Data on the input lines (D_0 - D_3) is stored at the low-to-high transition of the CLOCK line. A low signal on the CLEAR line will clear the register.

2235-15

Figure 5-1. Integrated Circuit Diagrams (Sheet 2 of 2)

Table 5-4. Universal Interface PCA (12930-60001) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
	12930-60001	UNIVERSAL INTERFACE PCA	28480	12930-60001
C1, C 3 thru C22, C24 thru C27, C29 thru C42, 44, 46,47	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw	56289	C023F101F1032 S22-CD
C2, 23, 48	0180-0197	CAPACITOR, fxd, elect, 2.2 μF, 10%, 20 Vdcw	56289	150D225X9020A2-DYS
C28	0160-3456	CAPACITOR, fxd, cer, 1000 pF, 10%, 250 Vdcw	56289	C067F251F102KS 22-CD
C43, 45	0160-2198	CAPACITOR, fxd, mica, 20 pF, 5%	28480	0160-2198
Q1	1854-0094	TRANSISTOR, Si, NPN	80131	2N3646
R1, 2, 35	0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416
R3, 4, 11, R26 thru R29,31,32	0757-0420	RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W	28480	0757-0420
R5, 6, 10, 13	1810-0075	RESISTOR, array, 7X750 ohms, 5%, 0.15W each	28480	1810-0075
R7	0757-0290	RESISTOR, fxd, flm, 6.19k ohms, 1%, 1/8W	28480	0757-0290
R8	0757-0401	RESISTOR, fxd, flm, 90.9 ohms, 1%, 1/8W	28480	0757-0401
R9	0698-4037	RESISTOR, fxd, flm, 46.4 ohms, 1%, 1/8W	28480	0698-4037
R12	0698-3156	RESISTOR, fxd, flm, 14.7k ohms, 1%, 1/8W	28480	0698-3156
R30	0698-0084	RESISTOR, fxd, flm, 2.15k ohms, 1%, 1/8W	28480	0698-0084
R33	0757-0280	RESISTOR, fxd, flm, 1k ohms, 1%, 1/8W	28480	0757-0280
R34	1810-0125	RESISTOR NETWORK (7 resistor 750 ohms 5%)	28480	1810-0125
U11, 13, 14, U21 thru U23, 31, 32, 41, 43, 44, 52	1820-0720	INTEGRATED CIRCUIT	28480	1820-0720
U12, 24, 42, 64, 74	1820-0788	INTEGRATED CIRCUIT, TTL	01295	SN35431
U15, 16, 34, 53, 54, 55, 65, 94, 104, 105, 114, 115	1820-1007	INTEGRATED CIRCUIT	28480	1820-1007
U17, 56	1820-0141	INTEGRATED CIRCUIT, TTL	04713	MC3001P
U25, 37, 76	1820-0626	INTEGRATED CIRCUIT, TTL	07263	U7B931459X
U26, 47, 67, 107	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7490N
U27	1820-0269	INTEGRATED CIRCUIT, DTL	04713	MC840P
U33, 95	1820-0839	INTEGRATED CIRCUIT, TTL	01295	SN35872
U35, 96, 103	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U36	1820-0328	INTEGRATED CIRCUIT, TTL	04713	SN7402N
U45	1820-0175	INTEGRATED CIRCUIT, TTL	01295	SN7405N
U46, 66	1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N
U50, 51	1990-0403	ISOLATOR, optically-coupled	28480	1990-0403
U57	1820-0372	INTEGRATED CIRCUIT, TTL	28480	1820-0372
U61 thru U63, U71 thru 73, U91 thru U93, 112, 113	1820-0721	INTEGRATED CIRCUIT, TTL	12040	SD14482
U75, 116, 117	1820-0515	INTEGRATED CIRCUIT, TTL	07263	U7B960259X
U77	1820-0511	INTEGRATED CIRCUIT, TTL	01295	SN7408N
U85, 87, 97, 102, 106	3101-1742	SWITCH, programmable, 3 pole, 10 position	28480	3101-1742
	3131-0251	STOP, switch	28480	3131-0251

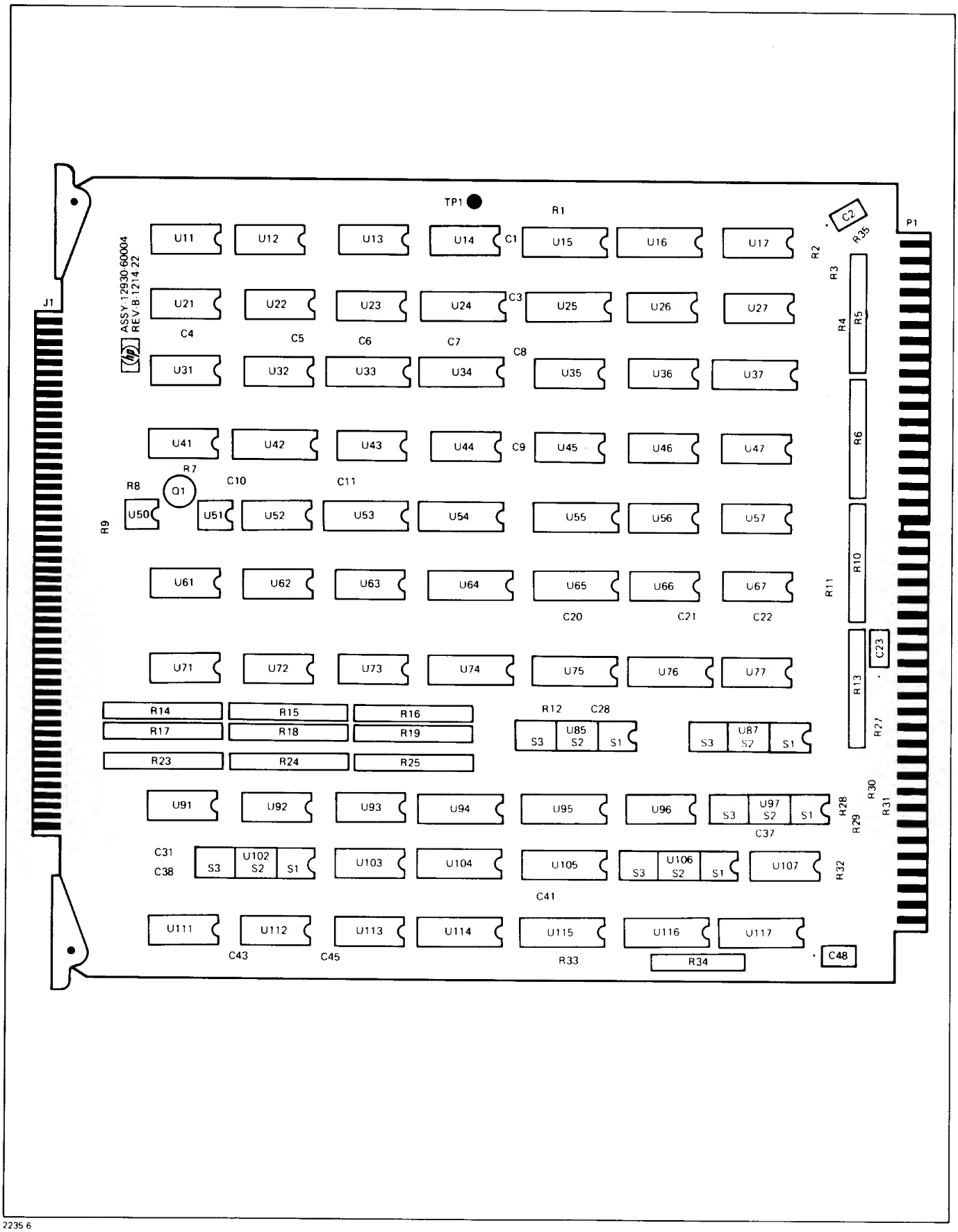


22355

Figure 5-2. Universal Interface PCA (12930-60001) Parts Location Diagram

Table 5-5. Universal Interface PCA (12930-60004) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
	12930-60004	UNIVERSAL INTERFACE PCA	28480	12930-60004
C1, C3 thru 11, C20 thru C22, 31, 37, 38, 41	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw	56289	C023F101F103ZS 22-CD
C2, 23, 48	0180-0197	CAPACITOR, fxd, elect, 2.2 μF, 10%, 20 Vdcw	56289	150D225X9020A2-DYS
C28	0160-3456	CAPACITOR, fxd, cer, 1000 pF, 10%, 250 Vdcw	56289	C067F251F102KS 22-CD
C43, 45	0160-2198	CAPACITOR, fxd, mica, 20 pF, 5%	28480	0160-2198
Q1	1854-0094	TRANSISTOR, Si, NPN	80131	2N3646
R1, 2, 35	0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416
R3, 4, 11, R26 thru R29, 31,32	0757-0420	RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W	28480	0757-0420
R5, 6, 10, 13	1810-0075	RESISTOR, array, 7X750 ohms, 5%, 0.15W each	28480	1810-0075
R7	0757-0290	RESISTOR, fxd, flm, 6.19k ohms, 1%, 1/8W	28480	0757-0290
R8	0757-0401	RESISTOR, fxd, flm, 90.9 ohms, 1%, 1/8W	28480	0757-0401
R9	0698-4037	RESISTOR, fxd, flm, 46.4 ohms, 1%, 1/8W	28480	0698-4037
R12	0698-3156	RESISTOR, fxd, flm, 14.7k ohms, 1%, 1/8W	28480	0698-3156
R14 thru R19, R23 thru R25	1810-0138	RESISTOR NETWORK (8 resistor, 330 ohms, 5%)	28480	1810-0138
R30	0698-0084	RESISTOR, fxd, flm, 2.15k ohms, 1%, 1/8W	28480	0698-0084
R33	0757-0280	RESISTOR, fxd, flm, 1k ohms, 1%, 1/8W	28480	0757-0280
R34	1810-0125	RESISTOR NETWORK (7 resistor 750 ohms, 5%)	28480	1810-0125
U11, 13, 14, U21 thru U23, 31, 32, 41, 43, 44, 52	1820-0720	INTEGRATED CIRCUIT	28480	1820-0720
U12, 24, 42, 64, 74	1820-0788	INTEGRATED CIRCUIT, TTL	01295	SN35431
U15, 16, 34, 53, 54, 55, 65, 94, 104, 105, 114, 115	1820-1007	INTEGRATED CIRCUIT	28480	1820-1007
U17, 56	1820-0141	INTEGRATED CIRCUIT, TTL	04713	MC3001P
U25, 37, 76	1820-0626	INTEGRATED CIRCUIT, TTL	07263	U7B931459X
U26, 47, 67, 107	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7490N
U27	1820-0269	INTEGRATED CIRCUIT, DTL	04713	MC840P
U33, 95	1820-0839	INTEGRATED CIRCUIT, TTL	01295	SN35872
U35, 96, 103	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U36	1820-0328	INTEGRATED CIRCUIT, TTL	04713	SN7402N
U45	1820-0175	INTEGRATED CIRCUIT, TTL	01295	SN7405N
U46, 66	1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N
U50, 51	1990-0403	ISOLATOR, optically coupled	28480	1990-0403
U57	1820-0372	INTEGRATED CIRCUIT, TTL	28480	1820-0372
U61 thru U63, U71 thru U73, U91 thru U93, 112, 113	1820-0721	INTEGRATED CIRCUIT, TTL	12040	SD14482
U75, 116, 117	1820-0515	INTEGRATED CIRCUIT, TTL	07263	U7B960259X
U77	1820-0511	INTEGRATED CIRCUIT, TTL	01295	SN7408N
U85, 87, 97, 102, 106	3101-1742	SWITCH, programmable, 3 pole, 10 position	28480	3101-1742
	3131-0251	STOP, switch	28480	3131-0251

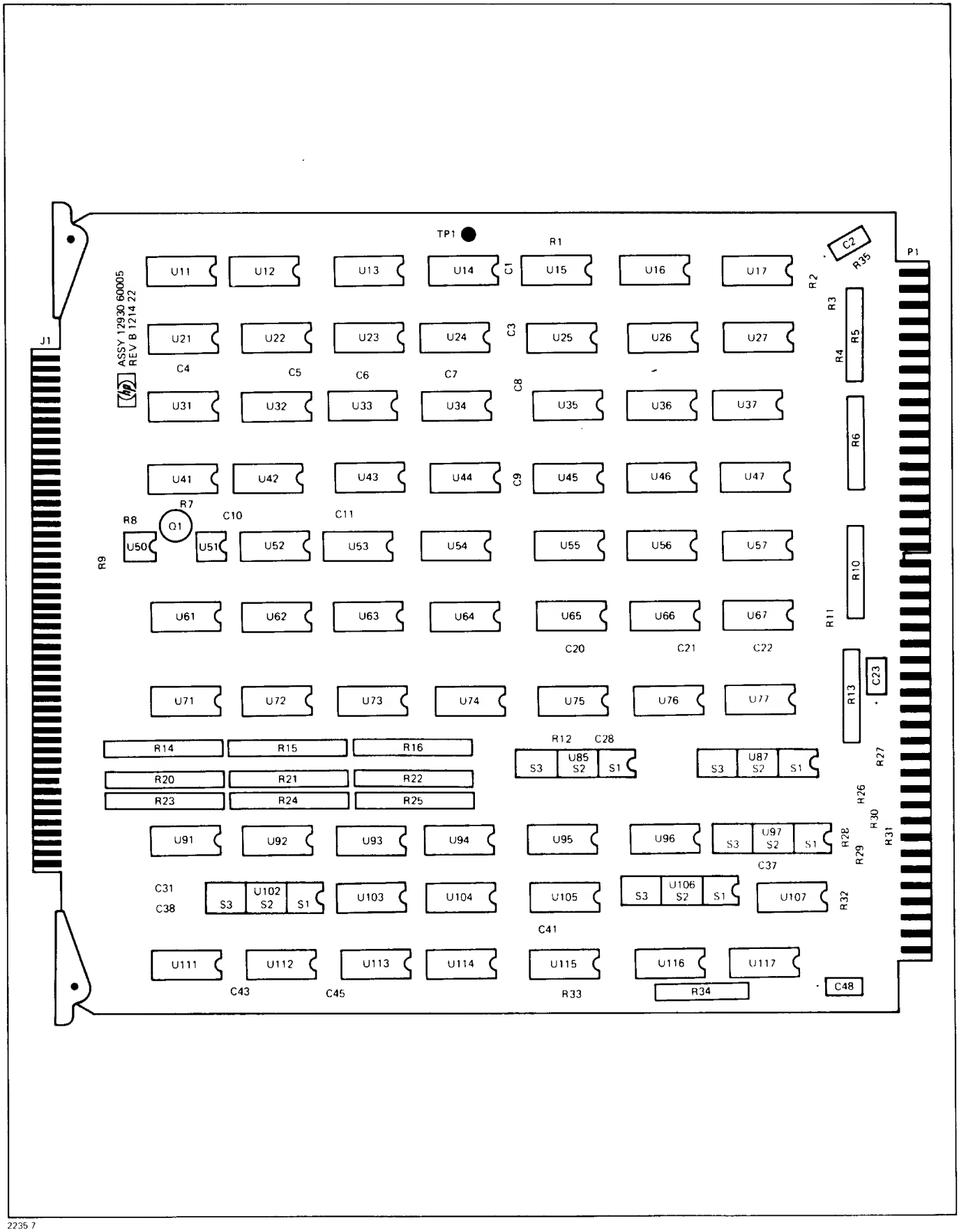


2235 6

Figure 5-3. Universal Interface PCA (12930-60004) Parts Location Diagram

Table 5-6. Universal Interface PCA (12930-60005) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
	12930-60005	UNIVERSAL INTERFACE PCA	28480	12930-60005
C1, C3 thru C11, C20 thru C22, 31, 37, 38, 41	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw	56289	C023F101F103ZS 22-CD
C2, 23, 48	0180-0197	CAPACITOR, fxd, elect, 2.2 μF, 10%, 20 Vdcw	56289	150D225X9020A2-DYS
C28	0160-3456	CAPACITOR, fxd, cer, 1000 pF, 10%, 250 Vdcw	56289	C067F251F102KS 22-C2
C43, 45	0160-2198	CAPACITOR, fxd, mica, 20 pF, 5%	28480	0160-2198
Q1	1854-0094	TRANSISTOR, Si, NPN	80131	2N3646
R1, 2, 35	0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416
R3, 4, 11, R26 thru R29, 31,32	0757-0420	RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W	28480	0757-0420
R5, 6, 10, 13	1810-0075	RESISTOR, array, 7 x 750 ohms, 5%, 0.15W each	28480	1810-0075
R7	0757-0290	RESISTOR, fxd, flm, 6.19k ohms, 1%, 1/8W	28480	0757-0290
R8	0757-0401	RESISTOR, fxd, flm, 90.9 ohms, 1%, 1/8W	28480	0757-0401
R9	0698-4037	RESISTOR, fxd, flm, 46.4 ohms, 1%, 1/8W	28480	0698-4037
R12	0698-3156	RESISTOR, fxd, flm, 14.7k ohms, 1%, 1/8W	28480	0698-3156
R14 thru R16, R20 thru R25	1810-0138	RESISTOR NETWORK (8 resistor, 330 ohms, 5%)	28480	1810-0138
R30	0698-0084	RESISTOR, fxd, flm, 2.15k ohms, 1%, 1/8W	28480	0698-0084
R33	0757-0280	RESISTOR, fxd, flm, 1k ohms, 1%, 1/8W	28480	0757-0280
R34	1810-0125	RESISTOR NETWORK (7 resistor 750 ohsm, 5%)	28480	1810-0125
U11, 13, 14, U21 thru U23, 31, 32, 41, 43, 44, 52	1820-0720	INTEGRATED CIRCUIT	28480	1820-0720
U12, 24, 42, 64, 74	1820-0788	INTEGRATED CIRCUIT, TTL	01295	SN35431
U15, 16, 34, 53, 54, 55, 65, 94, 104, 105, 114, 115	1820-1007	INTEGRATED CIRCUIT	28480	1820-1007
U17, 56	1820-0141	INTEGRATED CIRCUIT, TTL	04713	MC3001P
U25, 37, 76	1820-0626	INTEGRATED CIRCUIT, TTL	07263	U7B931459X
U26, 47, 67, 107	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7490N
U27	1820-0269	INTEGRATED CIRCUIT, DTL	04713	MC840P
U33, 95	1820-0839	INTEGRATED CIRCUIT, TTL	01295	SN35872
U35, 96, 103	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U36	1820-0328	INTEGRATED CIRCUIT, TTL	04713	SN7402N
U45	1820-0175	INTEGRATED CIRCUIT, TTL	01295	SN7405N
U46, 66	1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N
U50, 51	1990-0403	ISOLATOR, optically coupled	28480	1990-0403
U57	1820-0372	INTEGRATED CIRCUIT, TTL	28480	1820-0372
U61 thru U63, U71 thru U73, U91 thru U93, 112, 113	1820-0721	INTEGRATED CIRCUIT, TTL	12040	SD14482
U75, 116, 117	1820-0515	INTEGRATED CIRCUIT, TTL	07263	U7B960259X
U77	1820-0511	INTEGRATED CIRCUIT, TTL	01295	SN7408N
U85, 87, 97, 102, 106	3101-1742	SWITCH, programmable, 3 pole, 10 position	28480	3101-1742
	3131-0251	STOP, switch	28480	3131-0251



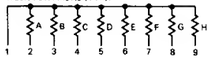
2235 7

Figure 5-4. Universal Interface PCA (12930-60005) Parts Location Diagram

UNIVERSAL INTERFACE (12930-60001, 12930-60004, 12930-60005, SERIES 1214)

NOTES:

1. RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS UNLESS SPECIFIED OTHERWISE.
2. *DENOTES COMPONENTS NOT USED ON TTL CIRCUITS.
3. SCHEMATIC DIAGRAM FOR RESISTOR PACKS (TYP):



4. P1 IS 86-PIN CONNECTOR INTERFACE TO COMPUTER.
5. J1 IS 100-PIN CONNECTOR INTERFACE TO I/O DEVICE.

DWG REV A
(SHEET 1 OF 2)

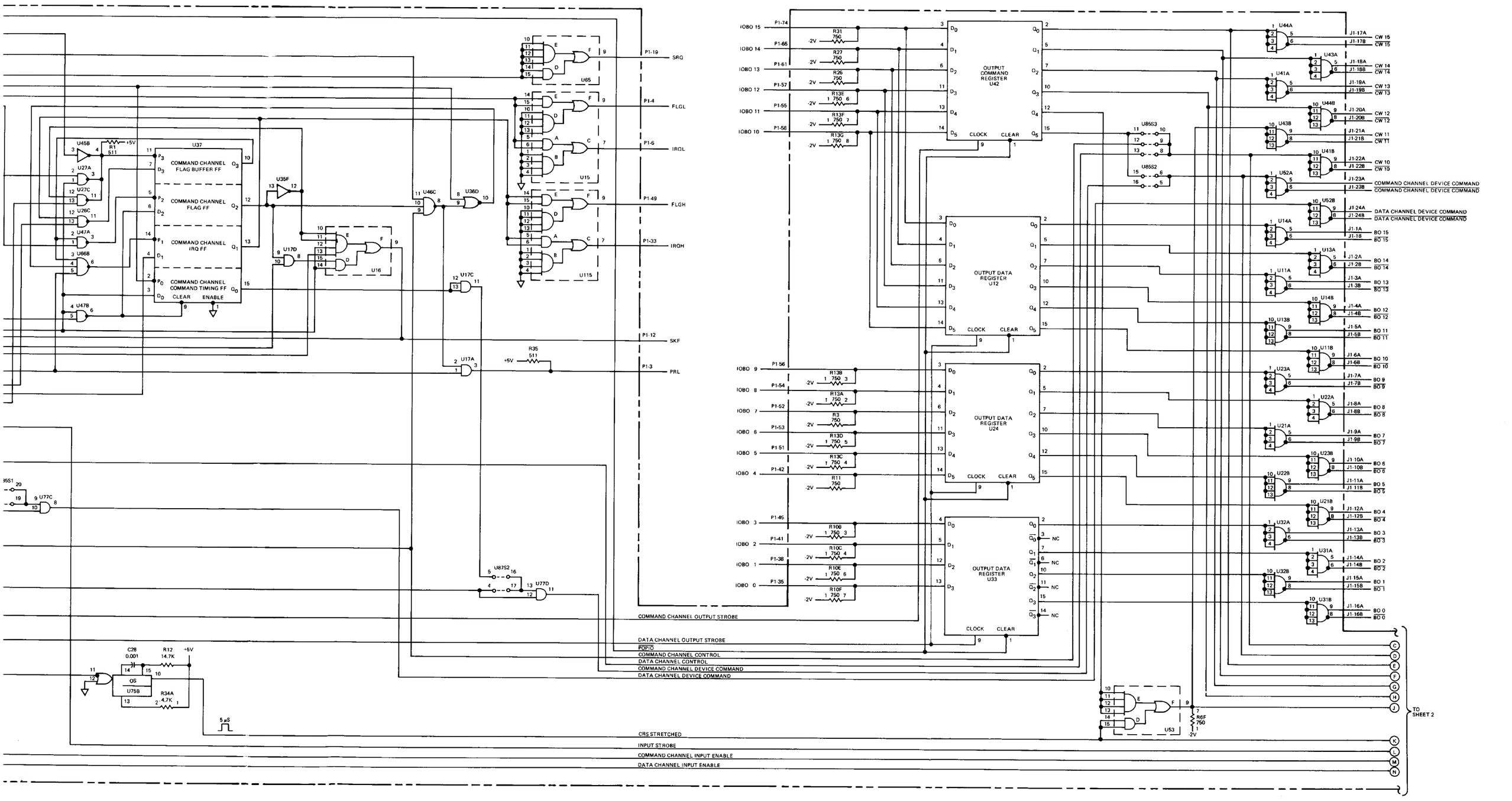


Figure 5-5. Universal Interface PCA Schematic Diagram (Sheet 1 of 2)

UNIVERSAL INTERFACE (12930-60001, 12930-60004, 12930-60005, SERIES 1214)

BIT 15 J1-26A → BIT 15
BIT 15 J1-26B → BIT 15
BIT 14 J1-27A → BIT 14
BIT 14 J1-27B → BIT 14
BIT 13 J1-28A → BIT 13
BIT 13 J1-28B → BIT 13
BIT 12 J1-29A → BIT 12
BIT 12 J1-29B → BIT 12
BIT 11 J1-30A → BIT 11
BIT 11 J1-30B → BIT 11
BIT 10 J1-31A → BIT 10
BIT 10 J1-31B → BIT 10
BIT 9 J1-32A → BIT 9
BIT 9 J1-32B → BIT 9
BIT 8 J1-33A → BIT 8
BIT 8 J1-33B → BIT 8
BIT 7 J1-34A → BIT 7
BIT 7 J1-34B → BIT 7
BIT 6 J1-35A → BIT 6
BIT 6 J1-35B → BIT 6
BIT 5 J1-36A → BIT 5
BIT 5 J1-36B → BIT 5
BIT 4 J1-37A → BIT 4
BIT 4 J1-37B → BIT 4
BIT 3 J1-38A → BIT 3
BIT 3 J1-38B → BIT 3
BIT 2 J1-39A → BIT 2
BIT 2 J1-39B → BIT 2
BIT 1 J1-40A → BIT 1
BIT 1 J1-40B → BIT 1
BIT 0 J1-41A → BIT 0
BIT 0 J1-41B → BIT 0

+4.85V: P1-39, P1-40 → +4.85V
C1, C3 THRU C11, C20, C21, C22, C31, C36, C37, C38, C41 0.01
C2, C48 2.2
TP1
GND: P1-1,2, P1-85,86
C23 2.2
-2V: P1-47, P1-48 → -2V

STS 6 J1-42A
STS 6 J1-42B
STS 5 J1-43A
STS 5 J1-43B
STS 4 J1-44A
STS 4 J1-44B
STS 3 J1-45A
STS 3 J1-45B
STS 2 J1-46A
STS 2 J1-46B
STS 1 J1-47A
STS 1 J1-47B
COMMAND CHANNEL DEV FLAG J1-48A
COMMAND CHANNEL DEV FLAG J1-48B
DATA CHANNEL DEV FLAG J1-49B
DATA CHANNEL DEV FLAG J1-49A
GND J1-50A
GND J1-50B
PON IN J1-25B
PON P1-66
PON OUT J1-25A

FOR POSITIVE-TRUE TTL, 12930-60005 ONLY

FOR GROUND-TRUE TTL, 12930-60004 ONLY

+5V
R23C 330 4
R25E 330 6
R24C 330 4
R24E 330 6
R23B 330 3
R23H 330 9
R24B 330 3
R24H 330 9
R25E 330 6
R25B 330 3
R23A 330 2
R23F 330 7
R24F 330 7
R24A 330 2
R25A 330 2
R25H 330 9
R20D 330 1
R21D 330 1
R20H 330 1
R21H 330 1
R19E 330 1
R22B 330 1
R17A 330 1
R20E 330 1
R21E 330 1
R22A 330 1
R19H 330 1
R17C 330 1
R18C 330 1
R17B 330 1
R18B 330 1
R19F 330 1

C32* 0.01 U91B
C34* 0.01 U92B
C39* 0.01 U111A
C40* 0.01 U112A
C47* 0.01 U113A
C42* 0.01 U111B
C44* 0.01 U112B
C43 20PF
C46* 0.01 U113B
C45 20PF

U102S3 U103A
U103D
COMD CHAN DEV FLAG COMPOSITE (A)
DATA CHAN DEV FLAG COMPOSITE (B)
U102S1
U102S2
U45D

+5V
R8 100
R7 6.17K
U50
U51
R30 2.15K
Q1

BIT 15 BIT 15 BIT 14 BIT 14 BIT 13 BIT 13 BIT 12 BIT 12 BIT 11 BIT 11 BIT 10 BIT 10 BIT 9 BIT 9 BIT 8 BIT 8 BIT 7 BIT 7 BIT 6 BIT 6 BIT 5 BIT 5 BIT 4 BIT 4 BIT 3 BIT 3 BIT 2 BIT 2 BIT 1 BIT 1 BIT 0

FOR POSITIVE-TRUE TTL, 12930-60005 ONLY

FOR GROUND-TRUE TTL, 12930-60004 ONLY

+5V
R16D 330 5
R16H 330 9
R15H 330 9
R15A 330 2
R14H 330 9
R14C 330 4
R16A 330 2
R16F 330 7
R15G 330 8
R15C 330 4
R14D 330 5
R14B 330 3
R16C 330 4
R16G 330 8
R15E 330 7
R15B 330 3
R14F 330 7
R14A 330 2
R16B 330 3
R16E 330 6
R15D 330 5
R15F 330 7
R14E 330 6
R14G 330 8
R25G 330 8
R25D 330 5
R24D 330 5
R24G 330 8
R23D 330 5
R23G 330 8
R25F 330 7
R25C 330 4
R22H 330 1
R21A 330 1
R20C 330 1
R22F 330 1
R21C 330 1
R20B 330 1
R22G 330 1
R21B 330 1
R20A 330 1
R22E 330 1
R21F 330 1
R20G 330 1
R19G 330 1
R22D 330 1
R21G 330 1
R20F 330 1
R22C 330 1
R19D 330 1
R18H 330 1
R17H 330 1
R19A 330 1
R17E 330 1
R19C 330 1
R18F 330 1
R17G 330 1
R19B 330 1
R18E 330 1
R17F 330 1
R19G 330 1
R18D 330 1
R17D 330 1
R19F 330 1

C13* 0.01 U63A
C12* 0.01 U62A
C14* 0.01 U61A
C19* 0.01 U63B
C17* 0.01 U62B
C15* 0.01 U61B
C18* 0.01 U73A
C16* 0.01 U72A
C24* 0.01 U71A
C27* 0.01 U73B
C26* 0.01 U72B
C25* 0.01 U71B
C30* 0.01 U93A
C35* 0.01 U92A
C33* 0.01 U91A
C29* 0.01 U93B

D_0 D_1 D_2 D_3 D_4 D_5
INPUT REGI U
CLOCK
+5V
INPUT REGI U
INPUT REG U
CLOCK
(L)

DWG REV A
(SHEET 2 OF 2) SEE SHEET 1 FOR NOTES.

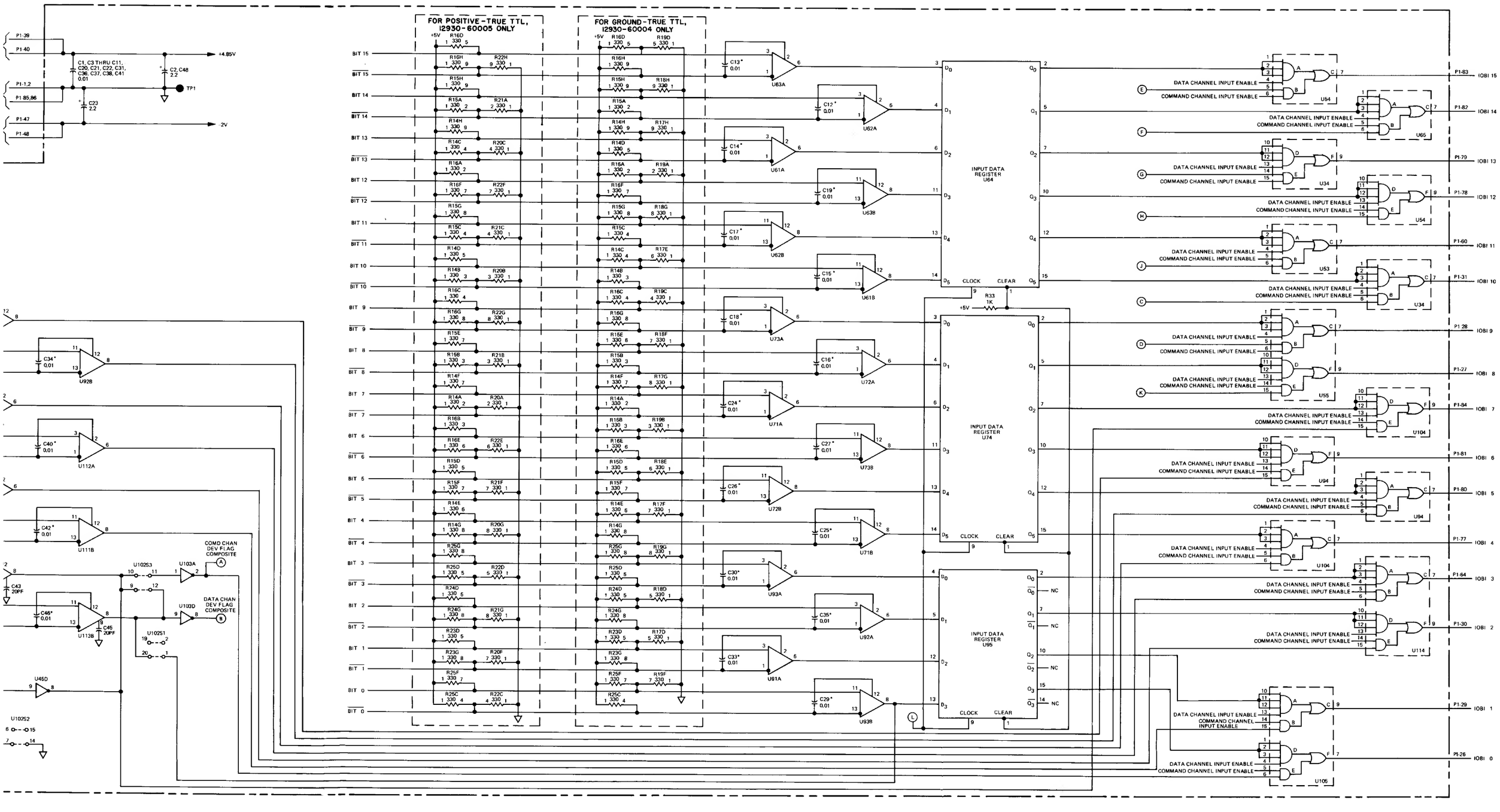


Figure 5-5. Universal Interface PCA Schematic Diagram (Sheet 2 of 2)

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION.

6-2. This section provides information for ordering replacement parts for the HP 12930A Universal Interface Kit. Separate parts lists and parts location diagrams are provided for each printed-circuit assembly in section V of this manual; parts listed in these tables are in alphanumeric order by reference designation. Table 6-1 is a numerical listing of parts for the interface kit.

6-3. Table 6-1 lists parts in numerical order by HP part number and lists the following information for each part:

a. Hewlett-Packard part number.

b. Description of the part. (Refer to table 6-2 for an explanation of abbreviations used in the DESCRIPTION column.)

c. Typical manufacturer of the part as a five-digit code. (Refer to table 6-3 for a listing of the manufacturers that correspond to the codes.)

d. Manufacturer's part number.

e. Total quantity of each part used in the kit.

6-4. ORDERING INFORMATION.

6-5. To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information for each part ordered.

a. Kit model number.

b. HP part number for each part.

c. Description of each part.

d. Circuit reference designation (if applicable).

Table 6-1. Numerical Listing of Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw	56289	C023F101F103ZS22-CD	42
0160-2198	CAPACITOR, fxd, mica, 20 pF, 5%	28480	0160-2198	2
0160-3456	CAPACITOR, fxd, cer, 1000 pF, 10%, 250 Vdcw	56289	C067F251F102KS22-CD	1
0180-0197	CAPACITOR, fxd, elect, 2.2 μF, 10%, 20 Vdcw	56289	150D225X902A2-DYS	3
0698-0084	RESISTOR, fxd, flm, 2.15k ohms, 1%, 1/8W	28480	0698-0084	1
0698-3156	RESISTOR, fxd, flm, 14.7k ohms, 1%, 1/8W	28480	0698-3156	1
0698-4037	RESISTOR, fxd, flm, 46.4 ohms, 1%, 1/8W	28480	0698-4037	1
0757-0280	RESISTOR, fxd, flm, 1k ohms, 1%, 1/8W	28480	0757-0280	1
0757-0290	RESISTOR, fxd, flm, 6.19k ohms, 1%, 1/8W	28480	0757-0290	1
0757-0401	RESISTOR, fxd, flm, 90.9 ohms, 1%, 1/8W	28480	0757-0401	1
0757-0416	RESISTOR, fxd, flm, 511 ohms, 1%, 1/8W	28480	0757-0416	3
0757-0420	RESISTOR, fxd, flm, 750 ohms, 1%, 1/8W	28480	0757-0420	9
1810-0075	RESISTOR, array, 7 x 750 ohms, 5%, 0.15W each	28480	1810-0075	4
1810-0125	RESISTOR NETWORK (7 resistor 750 ohms, 5%)	28480	1810-0125	1
1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7490N	4
1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N	2
1820-0141	INTEGRATED CIRCUIT, TTL	04713	MC3001P	2
1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N	3
1820-0175	INTEGRATED CIRCUIT, TTL	01295	SN7405N	1
1820-0269	INTEGRATED CIRCUIT, DTL	04713	MC840P	1
1820-0328	INTEGRATED CIRCUIT, TTL	04713	SN7402N	1
1820-0372	INTEGRATED CIRCUIT, TTL	28480	1820-0372	1
1820-0511	INTEGRATED CIRCUIT, TTL	01295	SN7408N	1
1820-0515	INTEGRATED CIRCUIT, TTL	07263	U7B960259X	3
1820-0626	INTEGRATED CIRCUIT, TTL	07263	U7B931459X	3
1820-0720	INTEGRATED CIRCUIT	28480	1820-0720	12
1820-0721	INTEGRATED CIRCUIT, TTL	12040	SD14482	12
1820-0788	INTEGRATED CIRCUIT, TTL	01295	SN35431	5
1820-0839	INTEGRATED CIRCUIT, TTL	01295	SN35872	2
1820-1007	INTEGRATED CIRCUIT	28480	1820-1007	12
1854-0094	TRANSISTOR, Si, NPN	80131	2N3646	1
1990-0403	ISOLATOR, optically coupled	28480	1990-0403	2
3101-1742	SWITCH, programmable, 3 pole, 10 position	28480	3101-1742	5
5040-6001	PCA EXTRACTOR	28480	5040-6001	2
8120-1895	CABLE	28480	8120-1895	25 ft
02116-6110	PRIORITY JUMPER PCA	28480	02116-6110	1
12930-60001	UNIVERSAL INTERFACE PCA	28480	12930-60001	1
12930-60006	TEST CONNECTOR ASSEMBLY	28480	12930-60006	1
12930-60007	KIT, cable hood	28480	12930-60007	1
	For Option 001, perform the following:			
	Delete the following entries:			
0160-2055*	CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw	56289	C023F101F103ZS22-CD	24
12930-60001	UNIVERSAL INTERFACE PCA (DIFF DRIVER)	28480	12930-60001	1
12930-60006	TEST CONNECTOR ASSEMBLY	28480	12930-60006	1
	Add the following entries:			
1810-0138	RESISTOR NETWORK (8 resistor, 330 ohms, 5%)	28480	1810-0138	9
12930-60004	UNIVERSAL INTERFACE PCA (GROUND-TRUE TTL DRIVER)	28480	12930-60004	1
12930-60008	TEST CONNECTOR ASSEMBLY	28480	12930-60008	1
	*Do not delete entire entry; change TQ entry to 18;			

Table 6-1. Numerical Listing of Replaceable Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
	For Option 002, perform the following:			
	Delete the following entries:			
0160-2055*	CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 Vdcw	56289	C023F101F103ZS22-CD	24
12930-60001	UNIVERSAL INTERFACE ASSEMBLY	28480	12930-60001	1
12930-60006	TEST CONNECTOR ASSEMBLY	28480	12930-60006	1
	Add the following entries:			
1810-0138	RESISTOR NETWORK (8 resistor, 330 ohms, 5%)	28480	1810-0138	9
12930-60005	UNIVERSAL INTERFACE PCA (POSITIVE-TRUE TTL DRIVER)	28480	12930-60005	1
12930-60009	TEST CONNECTOR ASSEMBLY	28480	12930-60009	1
	*Do not delete entire entry; change TQ entry to 18.			

MANUAL PART NO. 12930-90001
MICROFICHE PART NO. 12930-90003

PRINTED IN U.S.A.

HEWLETT PACKARD

12930A
UNIVERSAL INTERFACE KIT
OPERATING AND SERVICE MANUAL

UPDATING SUPPLEMENT

1 AUG 1974

MANUAL IDENTIFICATION

Manual Serial No. Prefix: NA
Manual Printed: Dec 1972
Manual Part No.: 12930-90001
Microfiche Part No.: 12930-90003

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to equipment containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Serial No. Prefix	Change
All (Errata)	1 thru 23

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Series	Changes

Changes 1 through 4 dated 20 July 1973.
Changes 5 through 7 dated 3 August 1973.
Changes 8 through 18 dated 18 June 1974.
Changes 19 through 23 dated 1 August 1974.

11000 Wolfe Road, Cupertino, California 95014, Tel. (408) 257-7000, TWX 910-338-0221
Europe: 1217 Meyrin-Geneva, Switzerland • Cable "HEWPACKSA" Tel. (022) 41.54.00

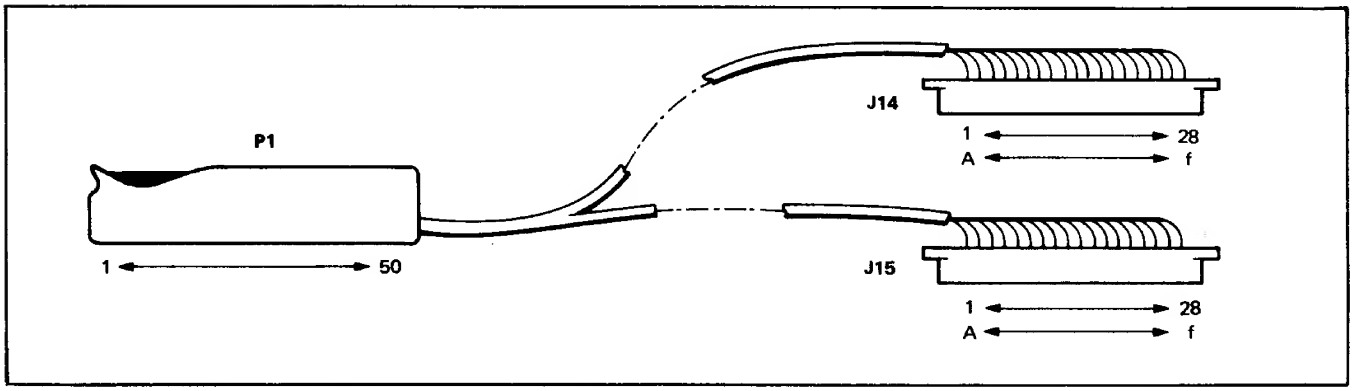
CHANGE	DESCRIPTION
1	Page 5-4, table 5-4. Change as follows: a. For HP Part No. 1820-0720, change Mfr Code from "28480" to "12040" and Mfr Part No. from "1820-0720" to "DM8830N." b. For HP Part No. 1820-1007, change Mfr Code from "28480" to "18324" and Mfr Part No. from "1820-1007" to "N8T23B." c. For HP Part No. 1820-0054, change Mfr Part No. from "SN7490N" to "SN7400N." d. For HP Part No. 1820-0269, change Mfr Code from "04713" to "01295" and Mfr Part No. from "MC840P" to "SN7403N." e. For HP Part No. 1820-0372, change Mfr Code from "28480" to "01295" and Mfr Part No. from "1820-0372" to "SN74H11N." f. For HP Part No. 1820-0721, change Mfr Part No. from "SD14482" to "DM8820AN."
2	Page 5-6, table 5-5. Perform change 1 above.
3	Page 5-8, table 5-6. Perform change 1 above.
4	Page 6-2, table 6-1. Perform change 1 above.
5	Page 2-1, table 2-1. In first entry under COMPUTER column, change to HP 2100A/S.
6	Page 2-4, table 2-3. Interchange functions for positions 5 and 6 of switch U106S2.
7	Page 2-5, table 2-4. Interchange functions for positions 1 and 2 of switch U87S1.
8	Title page. Change as follows: a. Printed-Circuit Assemblies: 12930-60001 (Standard), Series 1214 12930-60004 (Options 001 and 003), Series 1214 12930-60005 (Option 002), Series 1214 b. Add option 003 to "Options Covered" statement.
9	Page iii. Add the following tables: Title — Page 2-2A. Option 003 Interconnecting Cable Wire List . . . . . 2-3A 2-6. Programmable Switch Settings for Option 003 2-6
10	Page 1-1, paragraph 1-5. Add the following sentence at the end of paragraph 1-5: "Option 003 uses ground-true TTL drivers and is used to interface the computer to the HP 2894A Printing Reader Punch."
11	Page 1-1, table 1-1. Add Option 003 as follows: Option 003 12930-60004 12930-60008 12930-60012 02116-6110
12	Page 1-2, table 1-2. Under the heading "I/O Logic Compatibility", add Option 003 as follows: "Option 003: Ground-true TTL driver."
13	Page 2-1, paragraph 2-10. Change the first sentence to read as follows: "To maintain the universality of the interface kit, the interconnecting cable is supplied disassembled for the standard configuration and options 001 and 002. (Option 003 is supplied with a prefabricated cable assembly, part no. 12930-60012; an interconnecting

CHANGE	DESCRIPTION
13 (Cont)	cable wire list is provided in table 2-6A.) The disassembled cable permits user configuration according to specific need."
14	Page 2-2, paragraph 2-12. Delete third sentence and add the following: "For the standard interface kit and options 001 and 002, set the programmable switches as required according to the switch setting function definitions given in tables 2-3, 2-4, and 2-5. For option 003, set the switches as indicated in table 2-6."
15	Add new page 2-3A accompanying this supplement.
16	Page 2-6. Add table 2-6 as follows:

Table 2-6. Programmable Switch Settings for Option 003

PROGRAMMABLE SWITCH	POSITION
U85S1	2
U85S2	5
U85S3	0
U87S1	1
U87S2	4
U87S3	8
U97S1	1
U97S2	5
U97S3	0
U102S1	2
U102S2	7
U102S3	0
U106S1	2
U106S2	6
U106S3	9

17	Page 6-2, table 6-1: Change the entry "For Option 001, perform the following:" to read "For Options 001 and 003, perform the following:".
18	Page iii, list of illustrations. Add the following entry following figure 2-1: "2-2. Option 003 Interconnecting Cable . . . . 2-3B"
19	Add figure 2-2 (below) on a new page 2-3B.



7071-1

Figure 2-2. Option 003 Interconnecting Cable

Table 2-2A. Option 003 Interconnecting Cable Wire List

SIGNAL (AT PRINTING READER PUNCH)	INTERFACE PCA CONNECTOR	PRINTING READER PUNCH CONNECTOR	
	P1	J14	J15
Feed Request	23B	P	
Ready for Command	43B	W	
Secondary Hopper Select	17B		R
Punch	18B		N
Print	19B		P
Stacker Control Mode	20B	F	
Select Stacker (no. 2)	21B	J	
Separate Print Data	22B		J
Secondary Hopper Empty	47B		S
Card in Wait Station	44B	T	
Ready	42B	K	
*Load Output Buffer/New Data Request	24B	S	U
*Output Buffer Available/Print Buffer Available/Input Data Available	49A/27B	V	d/c
Clear Buffer Full	1B	R	
Input Buffer Full	26B/48B	U	
Read Check	29B	M	
Output Data 9	16B		Z
Output Data 8	15B		W
Output Data 7	14B		b
Output Data 6	13B		a
Output Data 5	12B		X
Output Data 4	11B		Y
Output Data 3	10B		e
Output Data 2	9B		f
Output Data 1	8B		A
Output Data 0	7B		B
Output Data 11	6B		H
†Output Data 12/Inhibit Input Feed	5B		V
Input Data 9	41B	c	
Input Data 8	40B	b	
Input Data 7	39B	d	
Input Data 6	38B	e	
Input Data 5	37B	f	
Input Data 4	36B	D	
Input Data 3	35B	B	
Input Data 2	34B	A	
†Input Data 1/Stacker Full	33B	N	
†Input Data 0/Primary Hopper Empty	32B	X	
†Input Data 11/Output Check	31B	a	
†Input Data 12/Input Check	30B	L	

NOTES:

1. *Indicates connected lines (OR-connection).
2. †Indicates time-shared lines.
3. All twisted pair returns are connected to pins 50A and 50B on connector A.
4. At connectors J14 and J15, each return wire of a twisted pair is connected to the pin on the opposite side of the connector which corresponds to the signal pin (for example, pins A and 1, f and 28, etc. are corresponding signal-return pins). (See figure 2-2.)

CHANGE	DESCRIPTION
20	Change 10 of this supplement. Change the name of the HP 2894A to read: "Card Reader Punch"
21	Change 13 of this supplement, the next to last sentence – table callout should read: . . . . . wire list is provided in table 2-2A.)
22	Page 2-3A, table 2-2A added by change 15 of this supplement. Make the following changes and additions: a. Change the name in the column heads from: PRINTING READER PUNCH, to: CARD READER PUNCH. b. In table 2-2A notes, correct the last part of NOTE 3 to read: . . . on connector P1. c. Add note 5 to the wiring table for option 003 as follows: 5. Capacitor C1 (.01 μFd, part no. 0160-0161) connects between pins 50B and 43A of P1, pins 26A thru 48A bus together, and a jumper from the bussed pins goes to 49B on P1.
23	Page 2-6, table 2-6 added by change 16 of this supplement. Change the Programmable Switch position callout for switch U97S2 from position 5 to position 6.